

# Highly Efficient UPS Topologies with Regenerated Switching Losses

Michael Frisch, Vincotech GmbH, Biberger Str. 93, 82008 Unterhaching (Germany)  
 Temesi Ernő, Vincotech Kft., Kossuth Lajos u. 59, H-2060 Bicske (Hungary)

High efficiency is a must for solar applications. Now other applications are emerging with equally challenging demands for efficiency. With the experience gained in high-efficiency solar applications, it is possible to exploit synergetic effects for next-generation UPS topologies. And in contrast to the solar market, system costs have been a focus topic from day one in this sector.

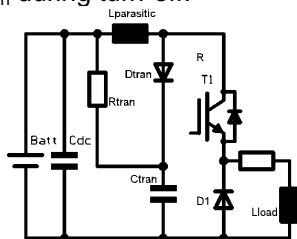
Switching losses have to be reduced to achieve higher switching frequencies and enjoy the size and weight benefits that passive components do not offer. Enhanced efficiency reduces the required battery capacity and cooling effort. Highly efficient circuits are clearly the smartest way to go for compact designs and highest power density. And the best news is that highest efficiency can be achieved at no extra cost – by means of parasitic inductance and intelligent integration into the UPS environment.

## 1 Regenerating switching losses

Low inductance allows engineers to use fast switches, but ultra fast freewheeling diodes are necessary to maintain low turn-on losses. The objectives here are to:

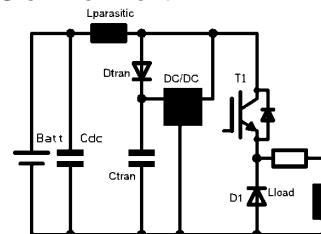
- Increase inductance at turn-on.
- Achieve ultra low inductance at turn-off.
- Regenerate the energy stored in the parasitic inductance:  $E_L = \frac{1}{2} * L * I^2$ .

The way to achieve this new switching behavior is to use the parasitic inductance  $L_{parasitic}$  at turn-on and bypass it during turn-off. To this end, the snubber diode  $D_{tran}$  (see Figure 1) consigns the parasitic inductance's stored energy to the integrated capacitor  $C_{tran}$  during turn-off.



**Figure 1: Asymmetrical inductance with feedback to the main DC link**

The stored energy circulates in  $L_{parasitic}$ ,  $D_{tran}$  and  $R_{tran}$  until it is dissipated in the parasitic resistor. With this circuit, we are able to spare the semiconductor switching losses. However, some energy has to be dissipated in passive components. One way to increase efficiency is to regenerate the stored energy using a DC-DC circuit (see Figure 2).



**Figure 2: Asymmetrical inductance with regenerated stored energy**

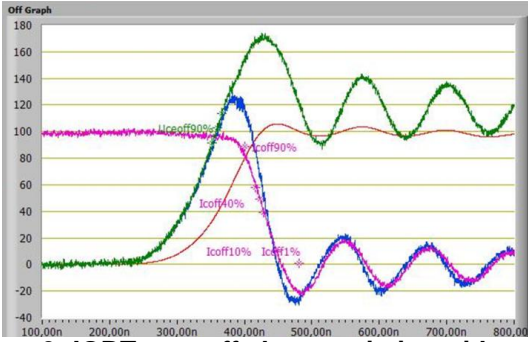
This proposal has been verified by comparing different parasitic inductances in a conventional power module setup and in an asymmetrical setup with integrated snubber capacitors.

Test conditions:

$R_G = 2\Omega$  (+/- 15V),  $V_{DC} = 600V$ ,  $I_{OUT} = 400A$   
 Component: Infineon HS3 / 1200V / 400A

### 1.1 Turn-off

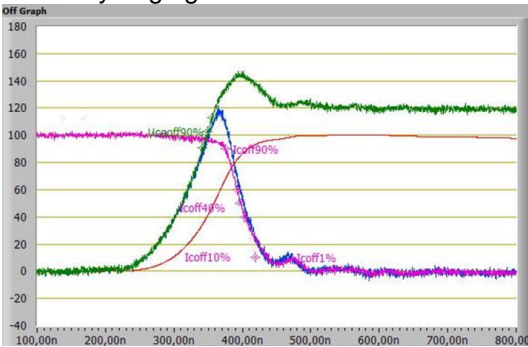
It is expected that the reduced inductance with integrated capacitors will decrease voltage overshooting at turn-off. The turn-off characteristic at a symmetrical inductance of 50nH (see Figure 3) indicates voltage overshoots >1000V and ringing with the DC capacitor.



**Figure 3: IGBT turn-off characteristics with symmetrical inductance;  $L[ON] = L[OFF] = 50nH$**

Turn-off at low temperatures is the most critical case. An overvoltage  $>180\%$  was measured at  $25^{\circ}C$ , which limits usage to  $650V$ . Safe turn-off is no longer possible given overcurrent conditions. In our test, the module failed at  $720A / 600V / T_J=25^{\circ}C$ .

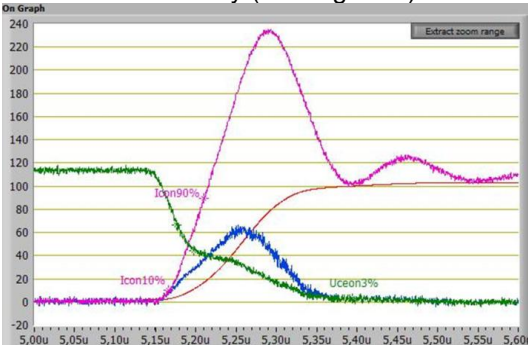
The same test with asymmetrical inductance (see Figure 4) confirms this expectation. The peak voltage is just  $720V$ , and the snubber diodes suppress any ringing



**Figure 4: IGBT turn-off characteristics with asymmetrical inductance;  $L[ON] = 50nH, L[OFF] = 5nH$**

## 1.2 Turn-on

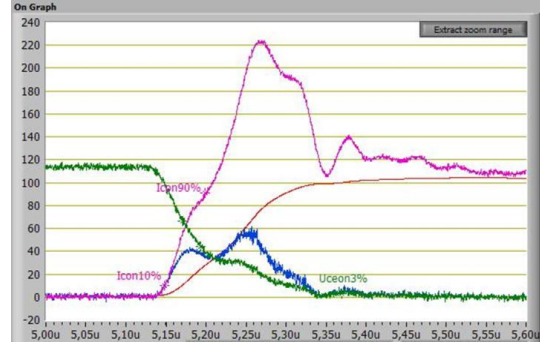
The freewheeling diode conducts when the IGBT is turned on with an inductive load. The reverse current is added to the output current in the IGBT during the diode's reverse recovery (see Figure 5).



**Figure 5: IGBT turn-on characteristics with symmetrical inductance;  $L[ON] = L[OFF] = 50nH$**

Asymmetrical inductance is similar, but the integrated capacitors do have some influence on the

freewheeling diode's reverse recovery (see Figure 6). At turn-on, the current of the transistor  $T_1$  is increased by the reverse recovery current through the diode  $D_1$ . The current is reduced at the end of the recovery phase, but additional energy is stored in the parasitic inductance  $L_{parasitic}$ . This causes an overvoltage at the transistor's collector. Some of the stored energy will flow into the capacitor, which reduces the reverse current in the diode and the forward current in the transistor. This significantly diminishes switching losses.



**Figure 6: IGBT turn-on characteristics with asymmetrical inductance;  $L[ON] = 50nH, L[OFF] = 5nH$**

Inductance may be further increased with the asymmetrical inductance circuit, and thereby take advantage of the reduced turn-on loss. The following table compares a circuit with a symmetrical inductance of  $50nH$  and two asymmetrical configurations with  $50nH$  (on) /  $5nH$  (off) and  $90nH$  (on) /  $5nH$  (off):

	Classic Lon/Loff = 50nH	Asymmetrical I Lon/Loff = 50nH/5nH	Asymmetrical II Lon/Loff = 90nH/5nH
$E_{OFF}$	27.78mJ	25.66mJ	25.77mJ
$E_{ON}$	16.92mJ	15.487mJ	12.44mJ
$E_{REC}$	31.78mJ	28.27mJ	26.70mJ
total	76.48mJ	69.42mJ (-10%)	64.91mJ (-15%)

The new asymmetrical setup's switching losses are lower. It is not just the turn-off losses that are reduced; all switching losses decrease.

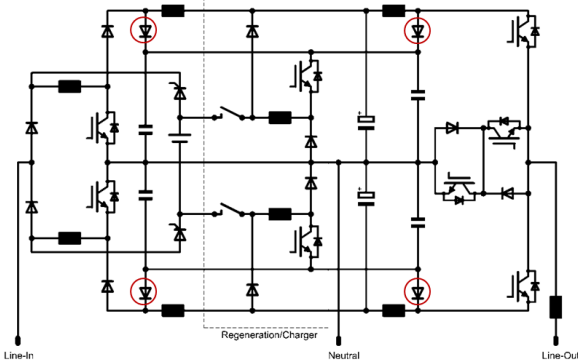
### This achieves several benefits:

- Superior switching performance with standard components:  
Reducing switching losses with standard components is entirely possible, so the new circuit improves efficiency without requiring investments in special components.
- Reduced EMI:  
The increased turn-on inductance reduces the peak current in the transistor, a major source of EMI.

- ❑ No bus bars required:  
Inductance in the DC input is now welcome and will further reduce losses at turn-on. Expensive laminated bus bars for a low inductive connection with the DC capacitor bank are no longer required. And that could well be this new design's greatest benefit.
- ❑ Reduced voltage swing of the onboard capacitors.  
The onboard capacitors are not discharged during turn-on, so voltage swing and dissipation in the capacitors are reduced.

## 2 Three-level UPS concept with regeneration

There is one problem left to solve before all these benefits can be enjoyed. The energy stored in the onboard capacitors has to be regenerated to maximize efficiency. This requires a symmetrical BUCK circuit. The same circuit is used in UPS systems to charge the battery. The idea here is to also use the battery charger to regenerate switching losses without extra effort and cost (see **Error! Reference source not found.**).

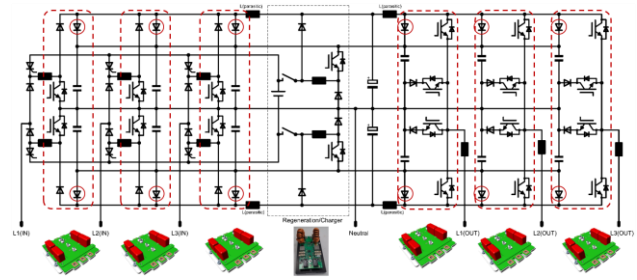


**Figure 7: UPS configuration (only 1 phase shown) with battery charger used for switching loss regeneration**

### 2.1 How this works:

- ❑ The energy stored in the parasitic inductance (PFC-DC and inverter-DC inductance) is transferred to the onboard snubber capacitors.
- ❑ The snubber capacitors of the input PFC and output inverter are connected.
- ❑ A diode prevents the capacitors from discharging reverse recovery current at turn-on.
- ❑ The snubber's stored energy is regenerated to the main DC voltage or used to charge battery.

All onboard capacitors are connected in the full-fledged three-phase UPS system (see Figure 8). A single central BUCK circuit charges the battery or regenerates the energy stored in the onboard capacitors back to the external DC link capacitor bank.



**Figure 8: Three-phase UPS configuration with a shared battery charger / switching loss regenerator**

### 2.2 This achieves several benefits:

- ❑ The parasitic inductance reduces the switch's turn-on losses without requiring an external low inductive DC connection.
- ❑ Reduced turn-off and turn-on losses:  
The onboard capacitor takes the parasitic inductance's stored energy at turn-off and after the BUCK diode's reverse recovery during turn-on.
- ❑ No extra effort:  
The snubber capacitor's stored energy is regenerated to the main DC voltage or charges the battery.

## 3 Power module definition

The combination of all these ideas has culminated in the following power module specifications.

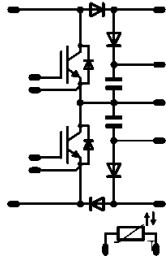
- ❑ 200kVA output power at 20kHz
- ❑ Asymmetrical parasitic inductance with energy regeneration.
- ❑ Three-level topology

## 4 Power module concept

The UPS concept is supported by dedicated power modules for input power factor correction (PFC) and the output inverter.

### 4.1 Input PFC module (see Figure 9)

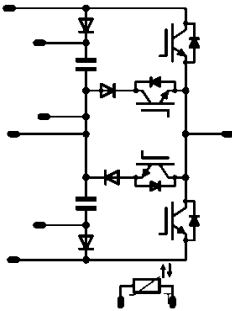
- ❑ 2x 650V / 600A power rating
- ❑ Asymmetrical parasitic inductance with onboard snubber capacitors (5nH turn-off inductance) and DC-DC regeneration circuit
- ❑ Symmetrical boost topology.



**Figure 9: Symmetrical boost circuit with onboard capacitors and interface for the regeneration of switching losses**

#### 4.2 Output inverter module

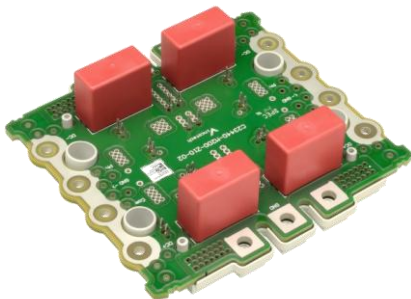
- ❑ 1200V / 600A power rating
- ❑ Asymmetrical parasitic inductance with onboard snubber capacitors (5nH turn-off inductance) and DC-DC regeneration circuit
- ❑ Split outputs in the high- and low-side circuit to decouple the corresponding switches
- ❑ Mixed voltage NPC (MNPC) topology



**Figure 10: Output three-level inverter module with onboard capacitors and interface for switching loss regeneration**

#### 4.3 Power module

The power module is equipped with DC snubber diodes and capacitors. Power feeds are connected via the screw terminals beside the capacitors. The contact holes alongside the module provide a low inductive interface for all DC voltages and connections for all switches.



**Figure 11: Power module mechanics with power connection and low inductive interface**

The following configurations are possible with this low inductive access to all IGBTs are:

- ❑ The three modules' transient DC path may be connected to access full capacity for all switches.
- ❑ Paralleled modules:  
The transient interface supports each switch's low inductive paralleling.
- ❑ Extended capacitance:  
The ultra low inductive capacitance can be increased with additional capacitors connected at the low inductive interface. Each conversion stage gets full access to the entire onboard capacitance with the low inductive connection of the DC voltage between all modules (all three phases, input and output).
- ❑ Connected switching loss regeneration:  
Resistors or a symmetrical BUCK circuit may be connected to the transient interface to regenerate the energy stored in onboard capacitors.

## 5 Conclusion

Switching loss regeneration with asymmetrical inductance achieves great benefits without extra effort and cost. It can even serve charge batteries in UPS systems.

- ❑ No laminated bus bars are required for external interconnection. The parasitic inductance is used to reduce turn-on loss, while circumventing the voltage overshoot problem at turn-off.
- ❑ The snubber diode reduces voltage swing and losses in the onboard capacitors
- ❑ Reduced EMI and reduced pulse load for the external DC link capacitors:  
The snubber diodes suppress any ringing, and the increased turn-on inductance decreases the pulse current in the DC link.
- ❑ Increased efficiency and superior switching performance with standard components
- ❑ No extra effort for the regeneration circuit as it is also used for battery charging

## 6 References

- [1] Wilhelm Rusche and Marco Bässler: "Influence of Stray Inductance on High-Efficiency IGBT Based Inverter Designs," Infineon Technologies, Warstein, Germany 2010
- [2] Peter Haaf, Jon Harper: "Diode Reverse Recovery and Its Effect on Switching Losses," November 2006
- [3] Dr.-Ing. Paul Chr. Mourick: "Parasitic Inductivities and Parasitic Oscillations an Overview." Feb. 24, 2011
- [4] Temesi Ernő and Michael Frisch: "Power Module with Additional Low Inductive Current Path," Vincotech Germany and Hungary 2009
- [5] Temesi Ernő and Michael Frisch: "Asymmetrical Parasitic Inductance Utilized for Switching Loss Reduction in Power Modules," Vincotech Germany and Hungary 2012