

Power Module Design for an Ultra Efficient Three-Level Utility Grid Solar Inverter

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Abstract

The race to achieve highest efficiency had engineers turning to innovative topologies and new components such as SiC to take the lead. In parallel, after years of dormancy, old but very innovative ideas such as the mixed-voltage NPC topology have been rediscovered and put to good use in many solar inverter applications. Surprisingly, all these efforts have focused on the power range up to 100kW, while standard two-level topologies with low switching frequencies continue to dominate in the range beyond 100kW. The problem is that the extended geometry of high-power applications makes it difficult to avoid parasitic inductance. On top of that, the effect of parasitic components increases linearly with current. Most designs reduce switching speed to limit the influence of parasitic effects. And true enough, dynamic losses are indeed minimized when the switching frequency is reduced by up to 4kHz. The new power module design presented here transcends the limitations associated with >100kW power inverters to accommodate high switching frequencies and innovative topologies. Based on standard Si components, this new solution uses parasitic inductance and applies the fundamentals of power electronics to boost the performance of conventional designs.

1. Introduction

Parasitic effects such as stray inductance [7][8] and diodes' reverse recovery characteristics [5] are the main obstacles to achieving high switching frequencies for ultra high efficiency solar inverter applications ranging beyond 100kW. The overvoltage spike caused by parasitic inductance limits the turn-off switching speed. And increased turn-on switching speed comes at a high price - losses and increased electromagnetic interference (EMI) caused by the freewheeling diode's reverse recovery characteristics. The new power module design described here takes advantage of advances in power modules - for example, the three-level topologies used in low-power solar applications - and exploits this parasitic inductance to reduce turn-on losses. Parasitic inductance at turn-off can be bypassed with low-inductive transient current management. A special topology for paralleling MOSFET with IGBT is presented here to show how promising the prospects of this advanced new module design can be.

2. Switching Loss Reduction in 4 Steps:

Standard two-level inverters achieve around 95% efficiency at 16kHz, so a 200kW inverter will suffer about a 10kW loss. Power dissipation has to be reduced by 80% to achieve the targeted 99% efficiency. This can be done by minimizing switching losses in four 4 steps:

- ✓ **Step 1: Reduce the switched voltage with a three-level topology.**
- ✓ **Step 2: Use a low inductive design that accommodates fast components.**
- ✓ **Step 3: Achieve asymmetrical inductance, reduce turn-on losses and regenerate energy stored in the parasitic inductance.**
- ✓ **Step 4: Capitalized on the benefits of advanced paralleling.**

2.1. Why a Three-Level Topology? (Step 1)

Three-level topologies are certainly known for reducing switching losses, but this is not their only selling point. The reduced current ripple halves the output filter effort and losses at the same PWM frequency.

Definition of switching losses: $P_D = \int I_{CE}(t) * V_{CE}(t) * dt$

Reducing the switched voltage also reduces switching losses by 50% [2]. An additional reduction is possible because of the freewheeling diode's lower voltage rating. With the benefit of a mixed-voltage neutral clamped converter (MNPC) topology, the freewheeling diodes' voltage rating is just half that of a two-level half-bridge. The blocking voltage drops from 1200V to 600V (Figure 1). The 600V diodes' reverse recovery charge is much lower, which reduces turn-on losses. The total turn-on losses are calculated as the sum of the diode's reverse recovery losses and turn-on losses in the switch, which are also influenced by the freewheeling diode's recovery characteristics.

All this reduces total losses:

by 50% (turn-on and turn-off) with a three-level topology, and

by 30% to 60% (turn-on) with 600V diodes, depending on the switch's characteristics.

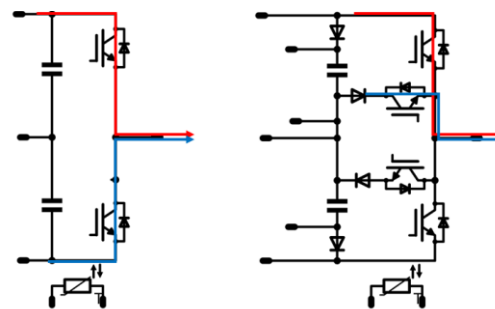


Figure 1: Switched current and freewheeling path in a two-level inverter vs. a three-level MNPC inverter during a positive half wave

2.2. Low Inductance for Fast Components (Step 2)

While fast diodes reduce turn-on losses, require fast switches a low-inductive design that solves the problem of voltage overshoot at turn-off:

$$V_{CE(peak)} = V_{CE} + L \times di/dt$$

High inductance precludes the use of fast components with high di/dt at turn-off. The overshoot dilemma increases with rising inductance (L) and switched current (I). Even lower inductance values are necessary to manage over-current and short-circuit problems. Reducing parasitic inductance also reduces voltage overshooting and turn-off losses. And it allows fast components to be used to accelerate turn-off, which is even more important to reducing switching loss.

All this can reduce total turn-off losses by around 20% to 60%. Acceleration at turn-on also depends on the diode.

2.3. Regenerating Energy Stored in the Parasitic Inductance (Step 3)

The low inductive design and fast components already reduce switching losses, and the low-inductive environment also allows us exploit parasitic effects to further reduce switching losses and improve EMC. Inductance is very welcome at turn-on. However, ultra-low inductance is vastly preferable at turn-off – hence the term *asymmetrical* inductance.

Asymmetrical Inductance at Work

The idea here is to make the most of parasitic inductance $L_{parasitic}$ at turn-on and avoid it altogether at turn-off (**Error! Reference source not found.**). To this end, the diode D_{tran} consigns the energy stored in the parasitic inductance to the integrated capacitor C_{tran} during turn-off.

The stored energy circulates in $L_{\text{parasitic}}$, D_{tran} and R_{tran} until it is dissipated in the parasitic resistor. Although we are able to relieve the semiconductor of switching losses with this circuit, some energy has to be dissipated in passive components. One way to increase overall efficiency is to regenerate energy stored in a DC-DC circuit (Figure 4).

Managing Energy Stored in the Parasitic Inductance

We want to regenerate the energy stored in the inductance, which otherwise has to be dissipated in the semiconductors. This stored energy is defined thusly: $E_{Lp}(I) = \frac{1}{2} * L_P * I^2$

Example for 350V/400A (turn-off): $E_{Lp}(400A) = \frac{1}{2} * 50nH * 400^2 = 4000\mu J$

Energy will also be transferred from the parasitic inductance into the on-board capacitor during turn-on, and the current will increase to:

$$I_L(\text{max}) = I(\text{output}) + I(\text{reverse recovery})$$

Energy generated by the reverse recovery current in the inductor will flow potentially into the capacitor.

With $I_{RR} = I_{Out}$: $E_{Lp}(400A) = \frac{1}{2} * 50nH * (400)^2 = 4000\mu J$

The potential power available for regeneration is:

$$P_S = f_{PWM} * (E_{LP-OFF} + E_{LP-ON})$$

$$P_S = 16kHz * (4000\mu J + 4000\mu J)$$

$$P_S = 128W \text{ per phase} = 384W \text{ for the 3 phase system.}$$

Sizing up the Onboard Capacitor

Energy stored in the parasitic inductance has to be transported to the onboard capacitor: $E_C = \frac{1}{2} * C * \Delta V_C^2$

The voltage increase is calculated as: $\Delta V_C = \text{SQR}(2 * E_C / C)$

Given the calculated example and an onboard capacitance of $6 * 680nF$, the voltage increase will be: $\Delta V_C = \text{SQR}(2 * 4000\mu J / 6 * 680nF) = 44.3V$

Therefore it is expected that a 44.3V increase will occur in the onboard capacitor at 400A output current.

Verifying Asymmetrical Inductance

A comparison of the different parasitic inductances in a conventional power module (Figure 2) and in an asymmetrical setup (Figure 4) with integrated snubber capacitors confirms that this idea is viable..

Test conditions: $R_G = 2\Omega$ (+/- 15V), $V_{DC} = 600V$, $I_{OUT} = 400A$
Component: IGBT-Highspeed / 1200V / 400A

Results with the conventional switching circuit ($L_{ON} = L_{OFF} = 50nH$):

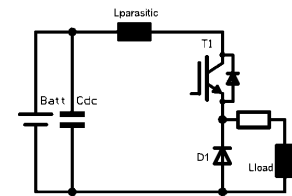


Figure 2: Conventional switching circuit with inductive load.

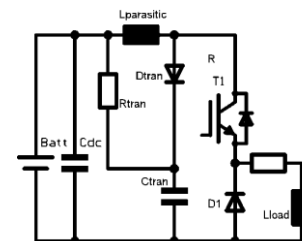


Figure 3: Current circulation in the asymmetrical inductance switching circuit with feedback to the main DC link

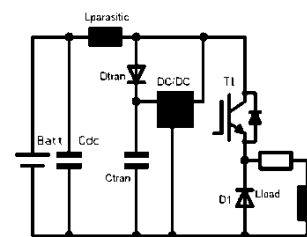


Figure 4: Asymmetrical inductance in a switching circuit with stored energy regeneration

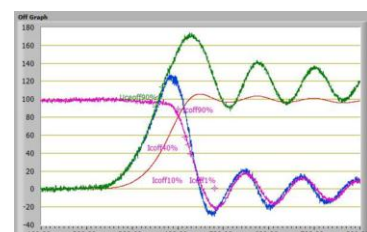


Figure 5: IGBT-Turn-Off characteristics with symmetrical inductance. $L[ON] = L[OFF] = 50nH$

$E_{ON}=16,92\text{mJ}$, $E_{OFF}=27,78\text{mJ}$, $E_{REC}=31,78\text{mJ}$

The voltage overshoot at turn off is about 180% at its peak (Figure 5). Clearly, over-current conditions rule out a safe turn-off!

The same measurement is now performed with an asymmetrical inductance (Figure 6) of 50nH at turn-on and 5nH at turn-off.

Results ($L_{ON} = 50\text{nH}$, $L_{OFF} = 5\text{nH}$):

$E_{ON}=15,487\text{mJ}$, $E_{OFF}=25,66\text{mJ}$, $E_{REC}= 28,27\text{mJ}$

The new asymmetrical setup's switching losses are lower. The overshoot at turn-off is minimized. Turn-off losses are lower. What's more, all switching losses are reduced. The circuit's reverse recovery behavior explains the lower turn-on losses. The reverse recovery current through diode D_1 boosts the current of transistor T_1 at turn-on. The current is reduced during recovery, but the additional energy stored in the parasitic inductance $L_{parasitic}$ causes an overvoltage at the transistor's collector, so the energy will flow into the capacitor. This reduces the reverse current in the diode. The voltage drops in the transistor, resulting in significantly reduced switching losses.

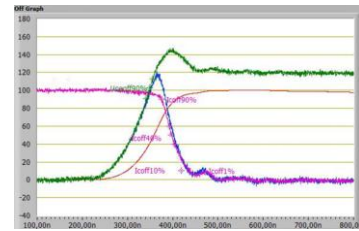


Figure 6: IGBT-Turn-Off characteristics with asymmetrical inductance. $L[ON] = 50\text{nH}$, $L[OFF] = 5\text{nH}$

Advantages of the Asymmetrical Inductance

- ✓ Superior switching performance with standard components: Increased turn-on inductance reduces peak current in the transistor, which is a major source of EMI.
- ✓ No laminated bus bars required: Increased inductance in the DC input is now welcome and will further reduce loss at turn-on. This means the expensive laminated bus bars used for a low inductive connection with the DC capacitor bank are no longer necessary.
- ✓ Reduced voltage swing of onboard capacitors: These capacitors are not discharged during turn-on, so their voltage swing and dissipation is drastically reduced. The transient diode eliminates any ringing between the DC link and the onboard snubber capacitors

Asymmetrical inductance reduces switching losses by 10% to 30%, depending on the parasitic inductance, while extending the safe operating range at turn-off (RBSOA).

2.4. Advanced Paralleling (Step 4)

The goal is to bring together the benefits of standard NPC (lowest switching losses) and mixed-voltage NPC (Figure 7A)[6] (lower static losses) topologies with a paralleled fast component (e.g. a MOSFET) and a component with low voltage drop (e.g. an IGBT) to create an advanced paralleled NPC topology (Figure 7B). This special circuit allows a 1200V IGBT to be paralleled with 600V MOSFETs.

This advanced paralleled NPC topology puts the inceptive idea of paralleling a MOSFET with an IGBT into action. Both the MOSFET and the IGBT are turned on simultaneously. The MOSFET is the faster device, so the current at turn-on flows to it. The IGBT turns on with low voltage. The voltage drop in the IGBT is lower, so then most of the current flows to the IGBT. The MOSFET's gate signal is delayed at turn-off. The IGBT turn off, and then the MOSFET takes over the current and turn off with a delay of $0.2\mu\text{s} \dots 1\mu\text{s}$.

To get access to those advantages are some challenges to

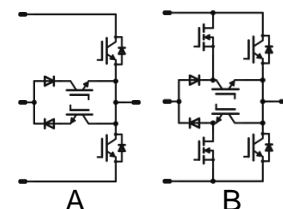


Figure 7: Mixed voltage NPC A and advanced paralleled NPC topology B

be solved:

- **Parasitic Turn-On**

The MOSFET turns off quickly, so the high dV/dt could send voltage into the paralleled IGBT's gate. It is already off, so this could trigger a parasitic turn-on. This problem is remedied with a negative gate bias and/or a capacitor inserted between the gate and emitter.

- **IGBT Tail Current**

Current flows to the MOSFET after the IGBT switches off. The IGBT turns off at zero voltage, but it will conduct again if the space charge region is not fully rebuilt. Turn-off efficiency will suffer as a result of this tail current. This problem is fixed by

1. Setting an ideal delay time between the IGBT and MOSFET
2. Selecting an IGBT with good zero-voltage turn-off behavior.

Measurements show that the advanced paralleled NPC topology halves switching losses (-50%).

3. A Power Module with Four Efficiency Improvements

Each of the four steps has been shown to be a viable improvement. And a module-based inverter solution proves how effective a combination of all four can be.

3.1. Power Module Definition (Figure 8, Figure 9)

- 3 Phase DC/AC inverter
- Low inductive module technology with onboard capacitors
- Asymmetrical inductance
- Interface for an external regeneration circuit.
- Advanced paralleled NPC topology
- Nominal current 400A
- Blocking voltage of the half-bridge IGBT and diode: 1200V
- Blocking voltage of the MOSFET and the components in the neutral path: 600V or 650V
- Split output
- External power connection with screw terminals

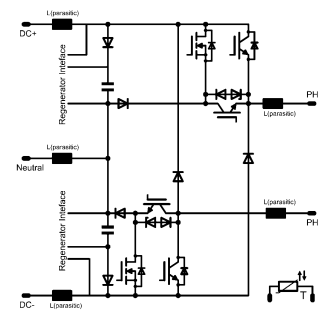


Figure 8: One phase of the 3-phase power module with advanced paralleled asymmetrical inductance, split output and regeneration interface

Figure 8 shows the inverter's circuit diagram (only one phase of three is shown). The inductance $L_{parasitic}$ in the schematic represents the power module's stray inductance.

Power Module

The power module (Figure 9) incorporates all power semiconductors of the inverter, the snubber diodes and the snubber capacitors. The circuit converts DC voltage from the solar panel into a three-phase AC voltage for the public power grid. The inductors shown in the DC path ($L_{parasitic}$) represent the parasitic inductance in the DC power module's connection.

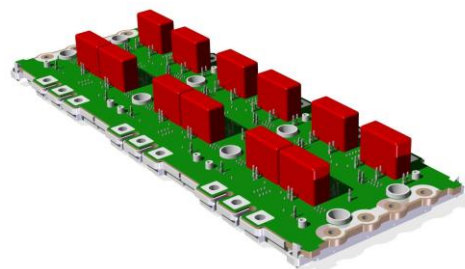


Figure 9: Power module (3 phase) with integrated snubber capacitors and asymmetrical inductance

The three-phase inverter circuit and the output filter (inductor) convert DC current into a sinusoidal output current. The regeneration circuit connected to the inverter module regenerates the energy stored in the onboard capacitors.

3.2. Measuring Switching Behavior (Figure 10)

It takes a special setup to measure switching behavior. Switched current cannot be measured from the outside because snubber capacitors are integrated inside the module, which is why the power module is equipped with a special measurement PCB (Figure 12). It affords access to all signals without influencing the low inductive connection between the switches and snubber capacitors.

The split output with PH+ for positive current and PH- for negative current allows switching measurements to be taken separately. Only the negative switching current is shown here. The Vcc positive supply represents the module's neutral connection. The measuring setup's GND is the module's negative supply, which allows high-frequency voltage signals to be measured on a grounded oscilloscope. Bridge_Low is the artificial parasitic inductance on the negative side. Snubber_Low is the artificial snubber capacitor on the negative side. The snubber capacitor is inserted between the module's transient negative connection and the DC supply's negative connection to measure high-frequency switched currents via current sensor I. VDC1 is a ground-independent HF floating capacitor bank. T6 is the negative side of the 1200V half-bridge IGBT. T4 is the negative side of the 650V NPC outer switch. T3 is the negative side of the 600V inner NPC switch. It is powered by batteries during the negative-current, real-power switching test.

Parallel Switch Optimization

The MOSFET and IGBT turn on simultaneously. The MOSFET is the faster device, so it takes on the turn-on losses. The IGBT is switched off first at turn-off; the MOSFET takes over the current and turns off after a short delay. Delay time is increased in 100ns increments until switching losses are minimized (Figure 11).

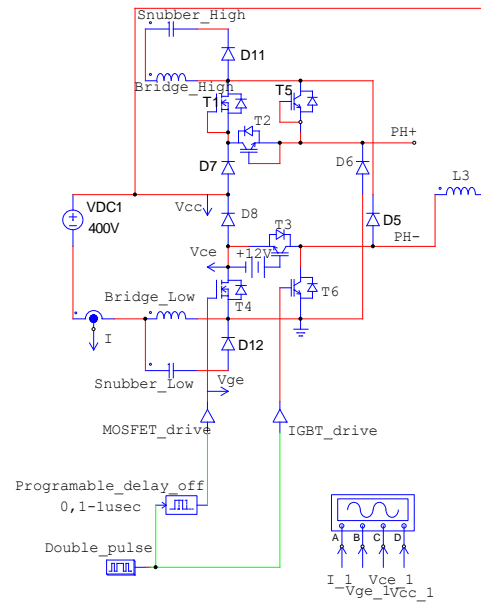


Figure 10: Schematics for switching characteristics measurement of the low side parallel switch and the freewheeling in the neutral path.

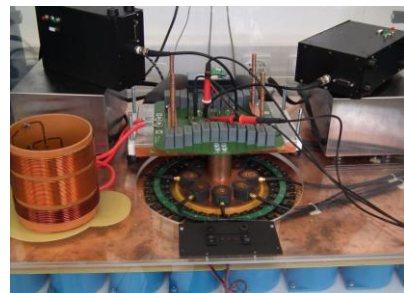


Figure 12: Test setup for dynamic characterization

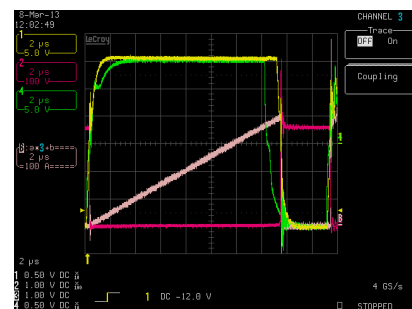


Figure 11: Turn-off gate signal; V_{GE} (IGBT): green
 V_{GS} (MOSFET): yellow
 V_{CE} : magenta

Turn-Off (Figure 13)

The turn-off inductance of $L_{OFF} = 10\text{nH}$ represents the module's inductance, which includes the snubber capacitors' internal inductance and the supply and current measurement loop's stray inductance. Fall time: $t_f < 18\text{ns}$, Sw. energy: $E_{OFF} = 7.5\text{mJ}$ (including 2mJ de-saturation loss during the $1\mu\text{s}$ delay) This results in practically ideal turn-off characteristics:

- ✓ Extremely fast fall time: $t_f < 18\text{ns}$
- ✓ Low turn-off inductance with $<120\text{V}$ voltage overshoot
- ✓ The snubber diodes suppress oscillation.
- ✓ Low turn-off energy. The turn-on energy of $E_{OFF} = 7.5\text{mJ}$ includes the increased static losses in the MOSFET during the $1\mu\text{s}$ delay time.

Turn-On (Figure 14).

- ✓ Rise time: $t_R = 40\text{ns}$,
- ✓ Switching energy: $E_{ON} = 4.5\text{mJ}$

The two steps shown in the graph in Figure 14 are explained by the high di/dt of the MOSFET. The 350V negative supply voltage on the negative parasitic inductance drops by $\Delta V = L \cdot di/dt = 25\text{nH} \cdot 400\text{A}/40\text{ns} = 250\text{V}$ => The devices receive just 100V during switching. After the 600V diode (D8) recovers at maximum current, both the MOSFET and IGBT are saturated and the voltage drops to zero.

3.3. Efficiency

The measured results serve to determine the efficiency of an inverter circuit. This calculation does not include losses of passive components such as the output filter and DC capacitors. The inverter achieves up to 99% efficiency at a PWM switching frequency of 16kHz , and about 98% at 64kHz (Figure 16).

4. Yet Another Efficiency Boost

Efficiency can be improved further by increasing turn-on inductance or using freewheeling 600V SiC diodes in the neutral path.

It is expected that the version with SiC diodes will reduce turn-on losses by around 30% to 50% (Figure 16).

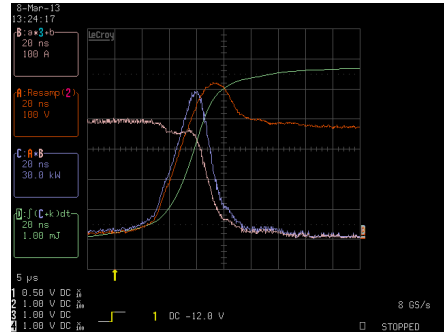


Figure 13: Turn-off characteristics.

Conditions: $T_J = 125^\circ\text{C}$, $I = 400\text{A}$, $V = 350\text{V}$

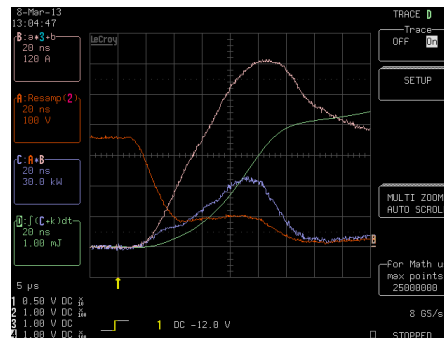


Figure 14: Turn-on characteristics.

Conditions: $T_J = 125^\circ\text{C}$, $I = 400\text{A}$, $V = 350\text{V}$, $L = 20\text{nH}$

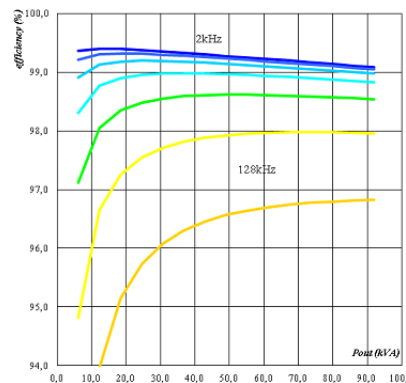


Figure 15: Advanced paralleled NPC:

Efficiency vs. switching frequency in steps from 2kHz to 128kHz : It doubles with each step – $2, 4, 8, 16\text{kHz}$ (blue), 32kHz (green), 64kHz (yellow), 128kHz (orange).

5. Conclusion

Conventional power designs can be improved by revisiting the fundamentals of power electronics.

- ✓ Multilevel topologies have been with us for many years to satisfy widespread demand for higher efficiency. This type of topology reduces switching losses by at least 50%.
- ✓ The low-inductive design ensures fast, reliable turn-off in high-current power modules and reduces voltage overshoot. Low inductive designs provide the platform for all other ideas about incorporating fast components, high transients and reduced switching losses in high-power applications.
- ✓ Asymmetrical inductance drives down switching losses, EMI and effort for inverter hardware. Low inductive bus bars are no longer necessary. A flexible, low-cost cable connection may be used in the DC link.
- ✓ The parallel switch technology achieves highest efficiency at elevated switching frequencies of 50kHz and beyond.
- ✓ Further improvements with SiC freewheeling diodes in the neutral path is feasible

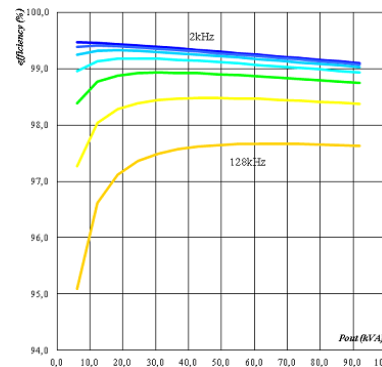


Figure 16: Estimated efficiency with SiC diodes in the neutral.

6. References

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