

Three-Level Topology for Single-Phase Solar Applications

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1 Abstract

Three-level topologies' enticing benefits are twofold: high efficiency and reduced filtering effort. Several multi-level topologies for single-phase solar applications are already on the market. This paper presents a new alternative, H6.5, briefly discusses operating principles, and benchmarks H-bridge, H6.5 and HERIC[®] topologies for efficiency and cost. In closing, it briefly describes the features of the new *flow*PACK 1 H6.5 modules.

2 The Idea Behind Three-level Topology

The sinusoidal output current generated by solar inverters is fed to the grid, where H-bridge topology with PWM (pulse width modulation) and an output filter produce sinusoidal output current. The main drawback of this two-level operation is that it requires a relatively large output filter and regenerates energy back to the DC capacitor during freewheeling. This regenerated energy flows to the inverter twice, which takes a toll on efficiency. Three-level topologies such as H6.5, in contrast, reduce filtering effort and switching losses. Fig.1 illustrates the idea behind this three-level operation. T11 and T14 switch on and energy flows to the output at active power. Energy then flows back to the DC capacitor through D13 and D12 during freewheeling, which compounds the losses within the system. Three-level topologies such as H6.5 and HERIC® uncouple the DC link capacitor from the AC output in the freewheeling phase to reduce overall losses.



Figure 1: The idea behind three-level operation



3 H6.5 Operating Principles and Topology Benchmarking

Fig.2 diagrams the innovative new H6.5 topology; fig.3 the HERIC[®] *topology.*





3.1 H6.5

The benefits, drawbacks and constrains of the two topologies at a glance: **Benefits:**

- Low static losses in the 3rd level operation:
 - ✤ Voltage drop at real power: 2 IGBTs
 - ✤ Voltage drop at freewheeling: 1 IGBT + 1 diode
 - Voltage drop at reactive power: 3 diodes
 - May also be used bidirectionally

Drawbacks:

- Complex structure: 6 IGBTs (4 ultra fast switching) and 5 fast diodes required
- Voltage drop at reactive power: 3 diodes (1 diode drop more)

3.2 HERIC[®]

Benefits:

- Low static losses in the 3rd level operation:
 - Voltage drop at real power: 2 IGBTs
 - Voltage drop at freewheeling: 1 IGBT + 1 diode
 - Voltage drop at reactive power: 2 diodes
 - May also be used bidirectionally

Drawback:

Complex structure: 6 IGBTs (4 ultrafast switching) and 6 fast diodes required

Constraint:

Patented topology

Figures 4 and 5 depict H6.5 and HERIC[®] topologies' operating principles with positive half-waves.





Figure 4: The operating principle of H6.5



Figure 5: The operating principle of HERIC[®]

We benchmarked H6.5, HERIC[®] and H-bridge topologies' cost and efficiency to allow for meaningful comparison and assessment, and included H-bridge topology to outline the differences between two-level and three-level topologies. Our efficiency calculation examined nominal and partial load scenarios at the power factors 1 and 0.8.

V _{inDC}	400V
V _{outRMS}	230V
I _{outnominal}	22.5A

Table 1: Simulation conditions

3.2.1 Benchmarking at Nominal Load

The charts in figures 6 and 7 compare the topologies' efficiency under nominal operating conditions. H6.5 and HERIC[®] clearly exhibit the same performance at a power factor of 1. Efficiency diverges by no more than 0.02% at a power factor of 0.8, but the lower cost compensates for this gap because H6.5 requires one less diode than HERIC[®]. The minimum efficiency gap between H6.5 topology and the H-bridge is 0.14% at 4 kHz. The gap widens as the switching frequency increases.





Fig. 6: Nominal load, pF: 1



Fig.7: Nominal load, pF: 0.8

3.2.2 Benchmarking at Partial Load

Partial load efficiency plays a key role in the weighted efficiency calculation for single-phase solar applications. European standards set out the following formula for calculating the weighted efficiency of a solar inverter:

Euro Efficiency= 0.03xEff5% + 0.06xEff10% + 0.13 xEff20% + 0.1x Eff30% + 0.48x Eff50% + 0.2xEff100%.

The California Energy Commission's weighted efficiency formula for a solar inverter is:

CEC Efficiency= 0.04xEff10% + 0.05xEff20% + 0.12xEff30% + 0.21xEff50% + 0.53 x Eff75% + 0.05xEff100%.



To compare topologies under partial load conditions, we ran simulations at 50% of nominal load, which has the biggest impact on the weighted efficiency calculation according to European standards. Figures 8 and 9 compare the topologies' efficiency at 50% of nominal load. H6.5 and HERIC[®] clearly exhibit the same performance at a power factor of 1. Efficiency diverges by no more than 0.02% at a power factor of 0.8, but the lower cost compensates for this gap because H6.5 requires one less diode than HERIC[®].



Fig. 8: Partial Load, pF:1



Fig.9: Partial load, pF: 0.8



3.2.3 Benchmarking for Cost

The solar market is price-driven. Even a small change in one component's price can have a big impact on the downstream system's cost. To get a better picture of these topologies' economics, we also benchmarked their costs. Fig.10 compares their normalized costs.



Fig.10: The cost benchmark

H-bridge topology requires just four IGBTs and four diodes, so it is, as expected, at the bottom of the price scale. HERIC[®] has one diode more for a total of twelve components and costs around 5% more than H6.5, which has eleven components. Fraunhofer-Gesellschaft holds the patent on HERIC[®], so royalties also have to be taken into account. This cost benchmark is meaningful for frequencies up to 20 KHz. Particularly in the H-bridge's case, it would take a bigger, costlier chipset to solve the problem of sharply increasing losses at higher frequencies.

4 Conclusion

The H6.5, a new three-level topology for single-phase solar inverters, is a viable alternative to solutions such as HERIC[®]. This new topology is suitable for real power and reactive power modes. The Vincotech *flow*PACK 1 H6.5 features this topology. It comes in 50 A, 75 A and 100 A versions with an IGBT S5 chipset in a *flow*1 housing. The module has LVRT (low voltage ride through) capability and a chipset optimized for switching frequencies up to 25 kHz.

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