High Efficient Topologies for Next Generation Solar Inverter

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Efficiency is becoming increasingly important in power electronics. In many applications, developments are driven by the initiatives for reduced energy consumption. The technology leaders are inverter applications in the solar market, since in this sector higher efficiency leads to a direct payback. The maximum efficiency target introduces new requirements for the electronic topologies and the power electronics components. Examples of new 1~ and 3~ solar inverter topologies are presented. New ideas for cos(Phi) compensation and high efficient bi-directional inverter/converter options are discussed.

High Efficiency Solar Inverter Designs - Status and Background

The new approach in solar applications is design to efficiency, replacing the target of design to power. The goal for traditional power electronic designs is highest power per EUR or USD. This target is secondary in solar inverter applications, because here it is possible to sell not only the maximal output power but also the European Efficiency (EE) level [1]. In the EE definition, the levels are weighted for the different expected intensity of the sun light (Fig. 1). The highest quantified operation mode is the condition at 50% of the nominal power.
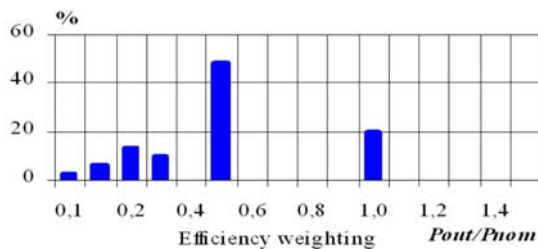

Fig. 1: European Efficiency (EE) weighting

To meet the required EE level for solar inverters, it is not enough to reduce the losses at nominal power; the efficiency at partial load is also critical. Thus, 'environmental friendliness' becomes a quantitative value which is easy to calculate:
Assuming EUR 4000 installation cost per kW [2] and a nominal power of 3kW, we get EUR 120 per 1% gained efficiency. In other words, it is better to spend more on some extra mm^2 silicon inside the power electronics rather than on some extra m^2 silicon of the solar panel on the roof.

Power Semiconductor Selection
The new design goal of highest efficiency leads to new selection criteria for the components used. In most Inverter topologies, the IGBT is the key component regarding cost and efficiency at maximum power. The nonlinear on-state voltage provides an advantage for the maximum power situation, but at partial power conditions this becomes a disadvantage. A MOSFET, with its linear behavior, achieves a better result at partial power. And with its superior dynamic characteristics it supports higher switching frequencies. The direct payback for efficiency enables the use of more expensive technologies, such as SiC diodes. SiC Schottky diodes reduce the switch-on losses in the transistor also minimizes EMC.

Design Goals for Solar Inverters
The design goals for the inverter in a transformerless topology are the following:

- Maximum power point (MPP) tracking of the solar panel for detection of the input voltage with the maximum input power
- Maximum EE for the inverter
- Low EMC

In order to run the inverter at the MPP, the circuit has to be able to adjust the input voltage according to the current light conditions. The MPP is usually at approximately 70% of the open loop voltage, but this is also dependent on the selected panel technology. Nevertheless, the input voltage has to be adjusted dynamically, for example with a boost circuit. In a 2nd stage, the DC-voltage has to be inverted into a sinusoidal grid-compatible voltage.

Topology for Transformerless 1~ Solar Inverter
The topology requirements also depend on the nominal power of the solar inverter. Up to approximately 4kW, single phase output inverters are usually used with a DC voltage of 500V max.
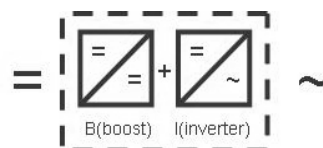

Fig. 2: Function blocks of a 1~ transformer less topology with boost + inverter function.

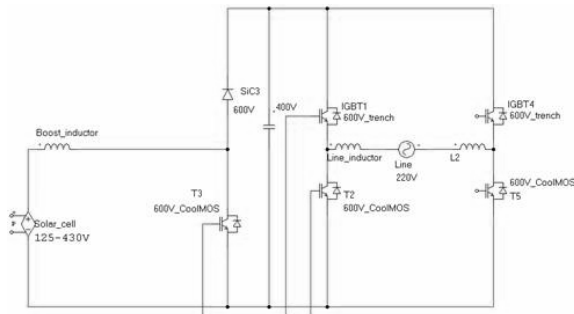These functional blocks (Fig. 2) are integrated in the following schematics (Fig. 3):

Fig. 3: Schematics of 1~ transformerless inverter topology

The booster adjusts the input voltage to the MPP. The output inverter injects the sinusoidal output current into the power grid. The high side IGBTs are used as polarity switches with 50Hz to reduce the losses and EMC in the output inverter. The low side IGBTs or MOSFETs are operated at PWM frequency. To keep the passive components of the boost inductor and of the output filter small, it is necessary to use a switching frequency of e.g. 16kHz.

The integration of the power semiconductors for this topology into a single module offers the following advantages:
- Easy and reliable assembly
- Fast design-in cycle => time to market!
- Better electrical behavior if the module design is conclusive.

For a conclusive module design the following issues are a must:
- Low induction in the DC.
  To achieve this target, the internal inductivity caused by wire bonding, layout and module pinning has to be minimized. This means the DC+ and DC– pins in the boost circuit as well as in the output inverter have to be placed as close to each other as the standards allow.
- Sense contacts for the fast-switching power transistors.
  The parasitic inductance of the wire bond at switch on/off of the IGBTs or MOSFETs will reduce the gate signal. This might cause oscillations in the transistor or at least increased switching losses. The currentless sense wire, bonded directly on the source or emitter pad of the transistor chip, will eliminate the problem. This is only possible with module technology.

Fig. 4 shows the Vincotech standard module flowSOL0-BI (P896-E01) which incorporates the advantages listed previously:
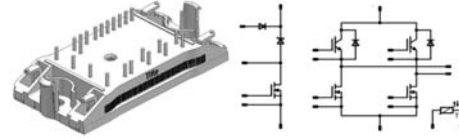

Fig. 4: flowSOL0-BI – boost circuit + mixed inverter.

Technical data:
- Boost circuit with MOSFET (600V/45mΩ) + SiC rectifier
- Bypass diode for maximum power (when exceeding nominal power)
- H-bridge with 75A/600V IGBTs + SiC Rectifier in the high side and MOSFET (600V/45mΩ) in the low side
- Temperature Sensor

Efficiency Calculation for Transformerless 1~ Power Module flowSOL0-BI
This paper only discusses the losses of the power semiconductors. The additional losses of the passive components, e.g. the boost inductor or output filter, are not considered.

A simulation based on measured values of this circuit shows the following results:
Conditions:
- P_{IN} = 2kW
- f_{PWM} = 16kHz
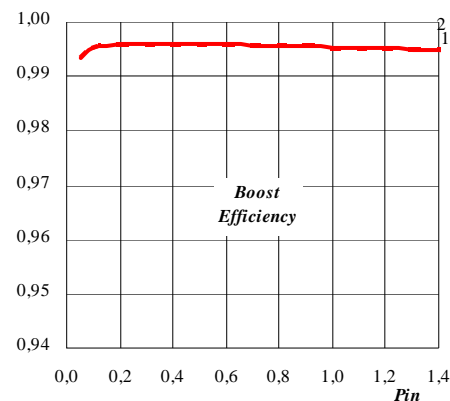- $V_{PV-nominal}$ = 300V
- V_{DC} = 400V

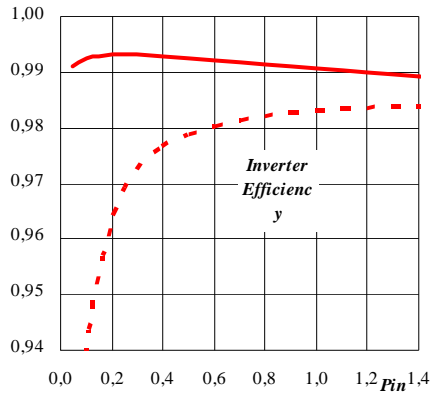Fig. 5: Simulation result for the boost circuit. => EE: 99,6%

Fig. 6: Simulation result for the output inverter => EE: 99,2% compared to 97,2% of a pure IGBT solution (dotted line)

The total EE for the module (booster + inverter) is 98,8%. This shows that a total efficiency, including the passive components, of 98% is reachable. Fig. 6 also shows that the efficiency of the alternative full IGBT solution drops significantly at partial load.

Topology for a Modular Transformerless 3~ Solar Inverter

Solar applications with higher power require three phase output and inputs for multiple solar strings (Fig. 7). The maximum DC voltage is increased to 1000V, which implies longer solar strings.
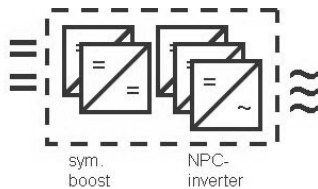

Fig. 7: Function blocks of a 3~ transformerless topology with boost + inverter function.

The standard output topology here is the 3~ output bridge, with a ½ bridge used as an inverter for each phase. This requires a maximum DC voltage of up to 1000V. The disadvantage is that components with a break-down voltage of 1200V are required, which tend to be slower than 600C components. The alternative is a neutral point clamped (NPC) inverter. With this topology, DC voltages of 1000V using standard 600V components are possible (Fig. 8).
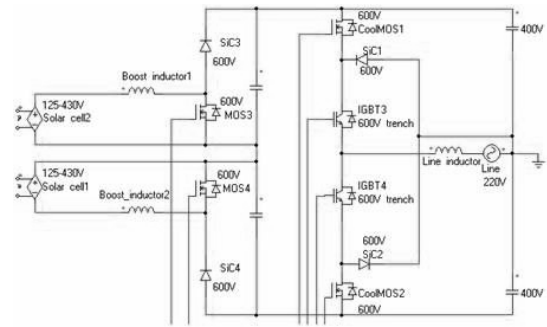

Fig. 8: Schematics of a solar inverter with NPC topology.

To achieve lowest parasitic inductance it makes sense to put the symmetrical boost circuit in one package and the NPC inverter circuit in a separate package.

Technical data symmetrical booster (Fig. 9):
- Dual boost circuit with MOSFET (600V/45mΩ) + SiC rectifier each.
- Bypass diode for maximum power (when exceeding nominal power)
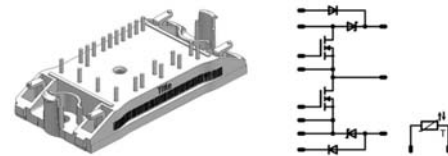- Temperature Sensor

Fig. 9: flowSOL0-NPB - symmetrical boost module

Technical data NPC-inverter (Fig. 10):
- 75A/600V IGBTs + fast rectifier in the center leg
- MOSFET (600V/45mΩ) in the outer leg.
- SiC rectifier for the neutral point connection
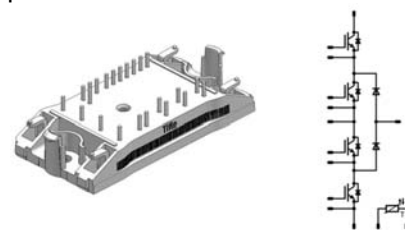- Temperature Sensor

Fig. 10: flowSOL0-NPI – NPC-inverter module

The same requirements regarding module design are valid here as mentioned in the 1~ solution. An additional requirement in this case is a low inductive design for the DC+, DC- and the NP.

With the aforementioned topologies, it is easy to combine e.g. 2 boost input modules with 3 output inverter modules (Fig. 11) to get a high efficient 10kW system. The pinning is defined in such a way that a further paralleling of the modules is simple.
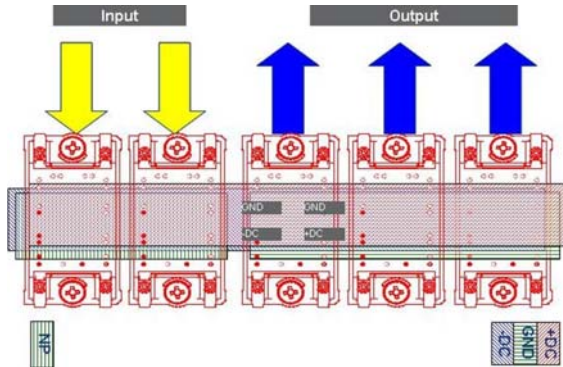

Fig. 11: Arrangement of 2 x Booster + 3 x NPC inverter modules

This topology achieves maximum efficiency for the current $1000V_{DC}$ designs. The comparison of the output inverter efficiency between the mixed (MOSFET+IGBT) and an IGBT Half-bridge with 1200V IGBTs (Fig. 12) shows the advantage of the mixed NPC inverter topology:
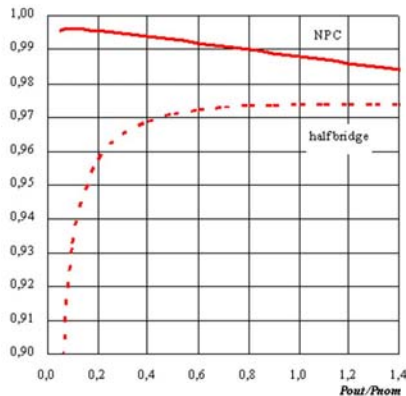

Fig. 12: Efficiency of a mixed NPC output stage (solid line) compared with an IGBT Half-bridge (dotted line)

The result for the weighted EE is 99,2% for the mixed NPC and 96,4% for the IGBT Half-bridge topology.

Ideas for the Next Generation Topologies

The mixed H-bridge topology already achieves a very high level of efficiency. In the following part, some ideas for further improvement of the following performance criteria are disclosed:

- Efficiency
- Reactive power

- High efficiency bi-directional conversion mode

Inverter Topologies for 1~ Output
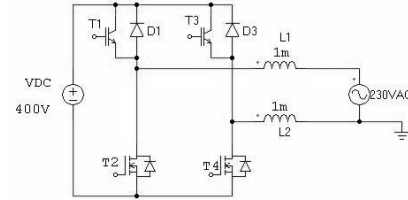The first focus is in improving the efficiency of the mixed H-bridge (Fig. 13).

Fig. 13: solar inverter stage - mixed

In the proposal in Fig. 13, the IGBTs are switched at the grid frequency (e.g. 50Hz) and the low side MOSFETs at a higher frequency of e.g. 16kHz PWM for a sinusoidal supply of the power. The simulation shows an EE of the inverter module of 99,2% at 2kW nominal power. MOSFETs cannot be used as high sides because of the slow intrinsic diode of the MOSFET.

As the high side is switched only with 50Hz, it is not necessary to filter the signal along this path. This is achieved with the open Emitter topology (Fig. 14), where only the HF-signal is filtered. This reduces the losses in the output filter.
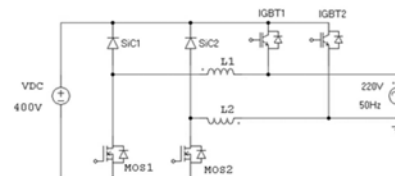

Fig. 14: Improved transformerless solution with open emitter in the highside

This new topology is already supported in a standard power module. The new Vincotech module (Fig. 15) flowSOL0-BI open E (P896-E02):
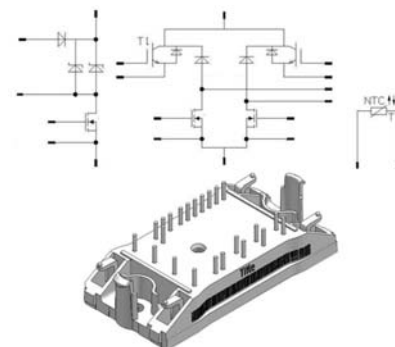

Fig. 15: flowSOL0-BI-open E (P896-E02)

Technical data:

- Boost circuit with MOSFET (600V/45mΩ) + SiC rectifier
- Bypass diode for maximum power (when exceeding nominal power)
- H-bridge with 75A/600V IGBTs + SiC Rectifier in the high side and MOSFET (600V/45mΩ) in the low side.
- Temperature Sensor

Let us have a closer look at the new topology (Fig. 15). During switching the low side MOSFETs, the anti-parallel diodes of the high side IGBTs are disabled with the inductor. This opens the possibility of using MOSFETs in the high side. The slow body diode of the MOSFET is disabled by the filter inductor, which improves the efficiency at low power. The simulation shows that at 2kW nominal power, the EE of the inverter is increased by 0,2% to 99,4%. In real life the improvement will be even higher, because in this simulation a constant chip temperature of 125°C is assumed. But as the MOSFET is oversized and, particularly at low power conditions, the chip temperature will be much lower, the R_{DS-on} will accordingly be lower.

What about reactive power? Dealing with a reactive load with this topology is only possible using FRED-FET, but these components usually have a higher Rds-on. Another disadvantage is that their bad reverse recovery properties lead to bad performance in the cos(Phi) compensation and bi-directional usage. If reactive power is not only necessary for line impedance measurement or for protection of the components at special conditions, the next topology (Fig. 16) could cover this issue.
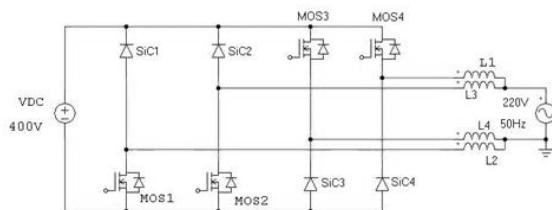

Fig. 16: Pure MOSFET solution suitable also for reactive load.

This circuit allows full reactive power and enlarges the use as a cos(Phi) compensation of the power grid and also for fully bi-directional applications, such as high efficiency battery chargers. An excellent efficiency level is reached in both directions when SiC Schottky diodes are used!

topology	Euro efficiency
pure IGBT	97,2%
mixed IGBT+MOSFET with SiC diodes	99,2%
pure MOSFET (open emitter) with SiC diodes	99,4%

Fig. 17: EE comparison at 2kW nominal power

Inverter Topologies for 3~ Output

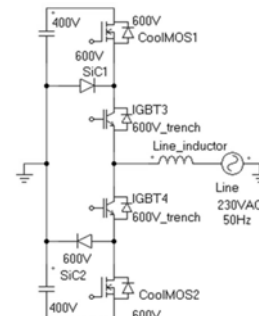Here a similar improvement for the NPC inverter is discussed.

Fig. 18: NPC inverter with mixed chip configuration

The NPC inverter (Fig. 18) reaches 99,2% EE at 2kW nominal power. With a small change it is possible to add the feature of reactive power.
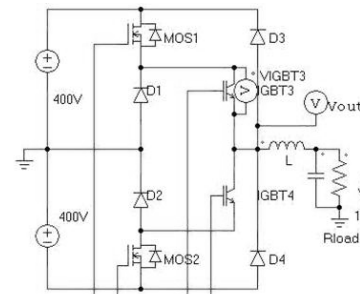

Fig. 19: NPC inverter with 2 x 1200V diodes in the output for reactive power option.

With 1200V diodes placed between output and DC, the topology is prepared for reactive power (Fig. 19). It would be also possible to design a bi-directional inverter with highest efficiency for the reverse conversion. For this purpose, SiC Schottky technology is recommended for the 1200V rectifier (D3, D4).

As such high voltage SiC diodes are very expensive, the following topology (Fig. 20) for high efficient compensation or bi-directional mode might be the better choice.
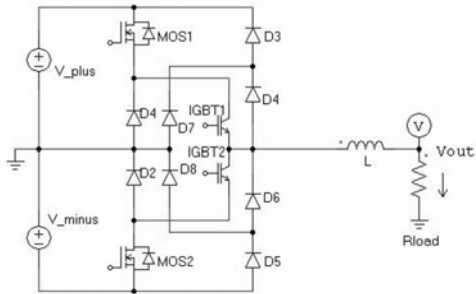

Fig. 20: NPC inverter with 2 x 600V SiC rectifier and 4 x Si diodes for reactive power option.

In this topology only 600V SiC Schottky diodes (D1, D2, D4, D6) are necessary. D3 and D5 are fast Si diodes and D7, D8 are small Si diodes to protect the rectifier from overvoltage.

Is it possible here to also make a pure MOSFET design? For this approach it is necessary to disable the body diode of the MOSFET. This is achieved with separate outputs and individual inductors for each of the output paths.
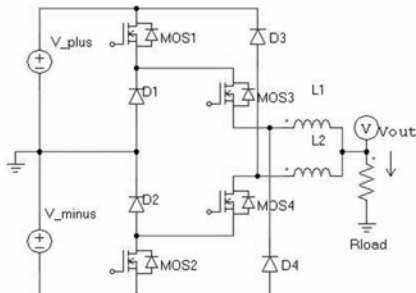

Fig. 21: NPC inverter with separated output and MOSFETs for all switches and 1200V diodes for reactive power option.

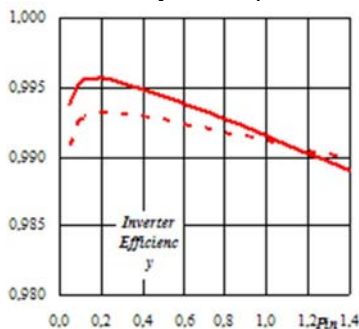With this circuit (Fig. 21) it is possible to increase the efficiency at low power.

Fig. 22: Efficiency of the NPC inverter at P_N=2kW with full MOSFET solution (solid line) compared to the mixed solution (dotted line)

The EE of the inverter module is increased from 99,2% to 99,4%. The reactive power is managed by fast 1200V diodes. SiC diodes are recommended here for maximum efficiency in the reverse direction. The alternative (Fig. 23) here is also the use of 600V SiC Schottky diodes (D1, D2, D4, D6) and 4 x 600V fast Si diodes:
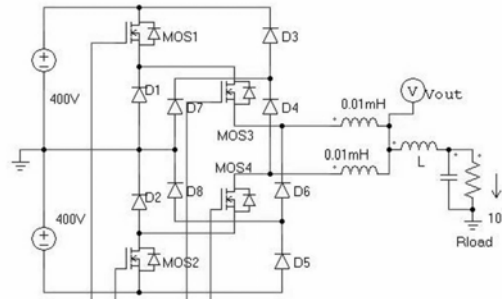

Fig. 23: NPC inverter with separated output with 600V SiC rectifier and 4 x Si diodes for reactive power option.

Conclusion

The new topologies open the possibility of scaling the efficiency of the inverter. As the efficiency maximum is reached already at 0.4KW, it is now possible to improve the system by paralleling of modules. An easy return of investment calculation will show which efficiency level makes sense in the application.

The capability to deal with reactive power will open this technology for new features and applications as:
- Cos(Phi)- line compensation
- High efficiency bi-directional battery charger for backup systems but also electrical vehicles and plug-in hybrid cars.
- high efficiency / high speed motor drive

References

[1] Martin Städler, Regenerative Energiesysteme \ PV \ System & Kosten ; 23.01.2008
[2] LOPEZ-POLO, Assun; MARKET DRIVERS FÜR NETZGEKOPPELTE PV-ANLAGEN IM INTERNATIONALEN VERGLEICH; Technische Universität Wien, Energy Economics Group. Gußhausstr. 25-29 / 373-2, A-1040 Wien