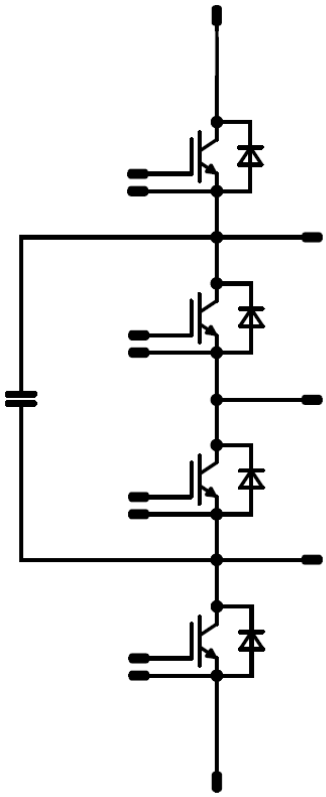
Vincotech

Flying Capacitor Inverter

The Advantages and Operation of Flying Capacitor Inverter



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1 Introduction

The demand for highly efficient solar inverters is steadily increasing in recent years. However, more cost efficient solutions are also desirable. Multi-level inverters are commonly used in PV applications. For the multi-level operation an adequate DC-link capacitor bank has to be utilized, which increases the cost, limits the lifetime and takes up a substantial footprint. The multi-level inverters are able to reduce the voltage stress on the semiconductors. Faster and cheaper semiconductors can be used with reduced EMI emission, and the voltage and current ripple are also reduced.Therefore the inductor size can be decreased. As compared to the two level inverter the semiconductor cost is higher, but the output filter is smaller and less expensive.

Let’s imagine that the advantages of two and three level topologies can be combined into a single inverter. The flying capacitor inverter combines low semiconductor costs and gives a multi-level output with high output frequency and low dynamic losses. Although the input is only two level with no need for the enormous DC-link capacitor bank, the output is multi-level and the output frequency is a multiple of the switching frequency. Therefore, the output filter can be reduced and slower semiconductors can be used.

2 The Flying Capacitor Inverter

In the flying capacitor topology the additional voltage levels are synthetized by high frequency capacitors, so-called flying capacitors. Here, the flying capacitors provides offset for the output, so the output voltage is the sum or the difference of the voltage levels. The schematic of the three level flying capacitor inverter can be seen in Figure 1. In the three level case the average voltage of the flying capacitor is half of the DC-link voltage.

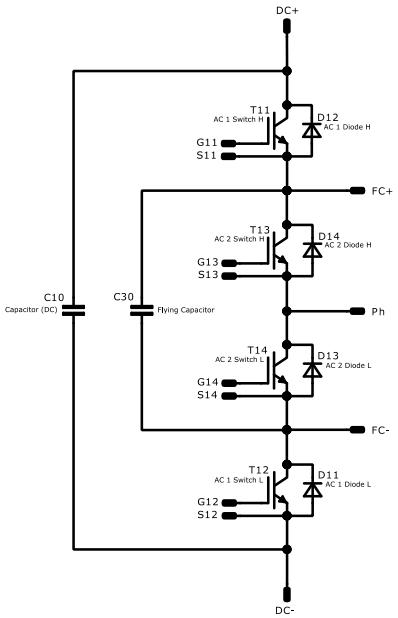


Figure 1: The three level flying capacitor inverter

2.1 The Commutation Loops

In flying capacitor inverter topologies the commutation loops include capacitors. A capacitor from the commutation point of view can be considered zero impedance. Its main role in the commutation loop is to offset the two outer semiconductors from each other. With this offset, the three level flying capacitor topology can be considered as two standalone half-bridges, where the outer one's commutation loop includes the DC-link capacitor, the outer diodes, the flying capacitor and the outer switches. The inner commutation loop includes the flying capacitor, the inner diodes and the inner switches. As the commutation loops are half-bridges, the loss calculation and the driving method are also similar for it (only the losses of the capacitors have to be added). The main constraint is also the same, all the two switches in each half-bridge must not be switched on at the same time. If all the two inner switches are switched on, the flying capacitor would be shorted. If all the outer switches are turned on the DC-link and the flying capacitor would be shorted, which can damage the inverter. The two commutation loops can be seen in Figure 2.

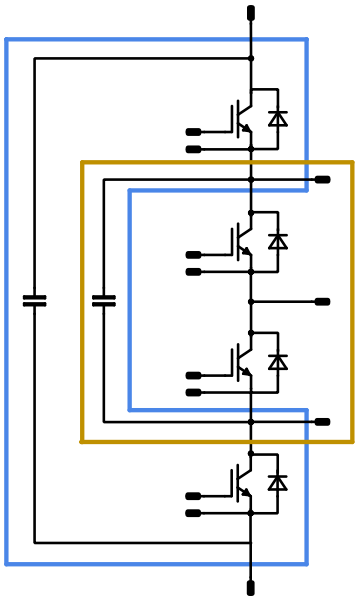


Figure 2: The commutation loops of the three level flying capacitor inverter

In general the number of voltage levels are theoretically endless, but in practice three, four and five levels are used. The additional levels in *n* level solution can be realized by adding extra outer commutation loops to the three level converter. Every added half-bridge's commutation loop will be similar to the blue loop in Figure 2. The number of voltage levels can be calculated as following:

$$n_{level} = p + 1$$

Where p is number of the commutation loops (half-bridges). The voltage of the capacitor can be calculated:

$$V_{FC,i} = V_{DC} \cdot \left(1 - \frac{i-1}{p}\right)$$

Where i is number of the given commutation cell. The first loop refers always to the most outer loop. $V_{FC,1}$ refers to the DC-link capacitor.

This application note covers the operation of the flying capacitor inverter. For easier understanding the three level version will be explained but the principles can be applied for any number of voltage levels.

2.2 Working Modes

Within the operation of the three level flying capacitor inverter four different modes can be derived. During normal operation the voltage of the flying capacitor is half of the output voltage and the inductor current is continuous. In the following chapter every mode is assumed with positive output current although the current direction is defined by the connecting circuitry. For easy reading the current direction on the semiconductors is also simplified. The conducting semiconductors (diode or IGBT) is always referred to the reference designator of the transistor. The reference frame of the neutral below is only valid if normal SPWM modulation is used. If the neutral point of the AC is not at the same potential as the half point of the DC supply (e.g.: third harmonic injection) the neutral of the DC has to be considered half of the DC supply. In Mode 1 DC+ is on the output. For that all the two upper transistor (T11 and T13) have to be switched on. This mode has no effect for the flying capacitor. Zero voltage can be synthetized on the output in two ways. In Mode two T11 and T14 are in ON state. In this case the voltage of the flying capacitor will be increasing. In Mode three T13 and T12 are switched on, so the capacitor voltage will be decreasing. The effect of Mode two and Mode three on the flying capacitor are depending on the output current direction. In case of negative current in Mode two the voltage of the capacitor will decrease, while in case of Mode three the capacitor will increase. In Mode four DC- can be switched by T12 and T14 to the output. Mode four does not affect the flying capacitor. The different modes can be seen in Figure 3 and Table 1.

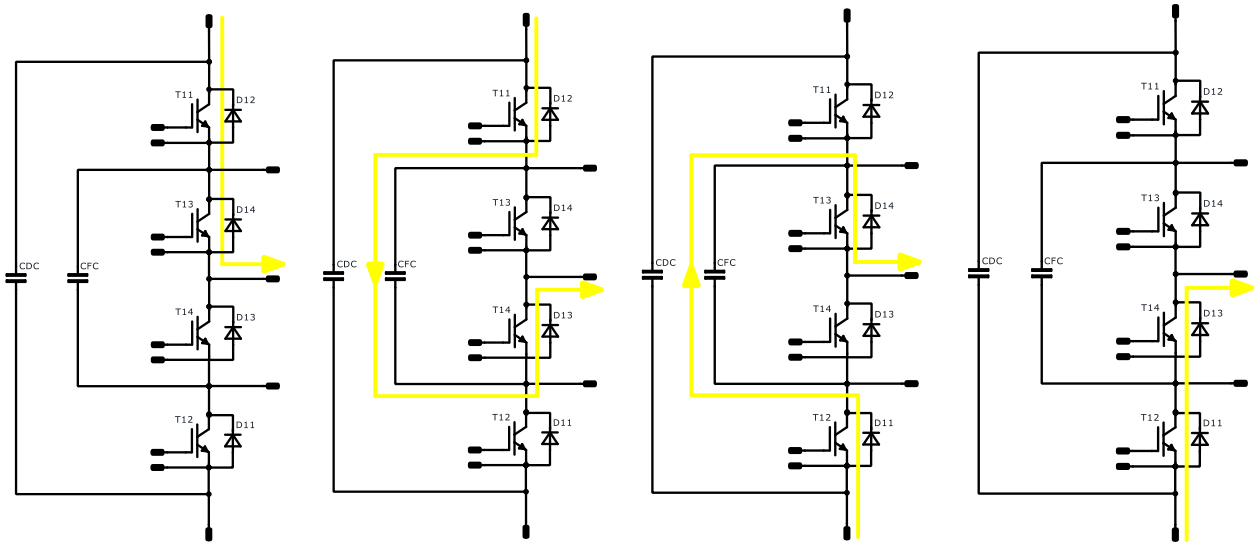


Figure 3: The operation modes of the flying capacitor inverter

Mode	Output	Transistors				FC voltage	
		T11	T13	T14	T12	Positive current	Negative current
Mode 1	DC+	ON	ON	OFF	OFF	No effect	
Mode 2	Neutral	ON	OFF	ON	OFF	Increasing	Decreasing
Mode 3	Neutral	OFF	ON	OFF	ON	Decreasing	Increasing
Mode 4	DC-	OFF	OFF	ON	ON	No effect	

Table 1: Output and FC voltage states

2.3 Operation of the Inverter

The driving method is the following: one of the half-bridge's drive signal have to be shifted 180° to the other. As this topology's driving is based on the half-bridge, the control signal of the low side has to be inverse of the high side. This results in the fact that the high and the low side cannot be switched on at the same time in one half-bridge (commutation loop).

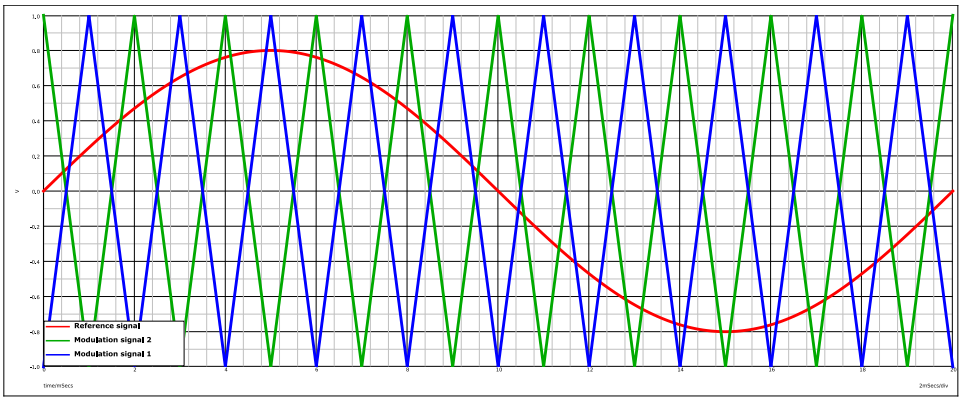
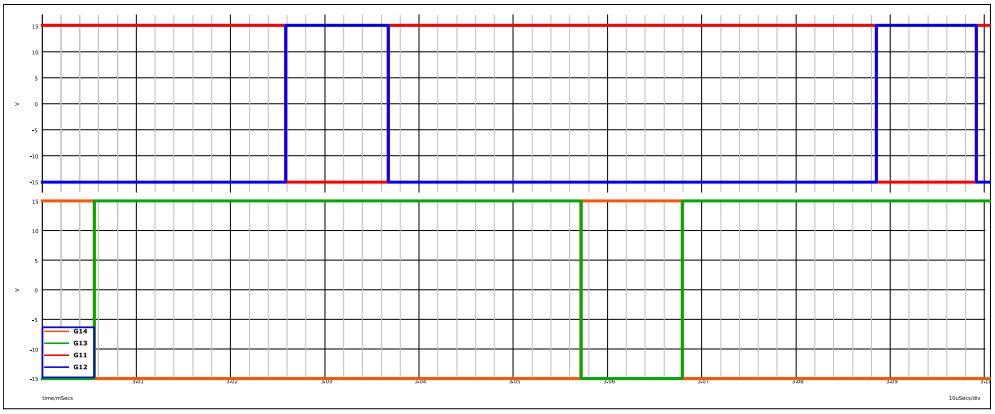


Figure 4: PWM signal generation

In Figure 4 the modulation signals and the reference signal can be seen. In Figure 5 the drive voltages, the flying capacitor voltage, the output and flying capacitor as well as the semiconductors voltages and currents can be seen with the same time step.

a)



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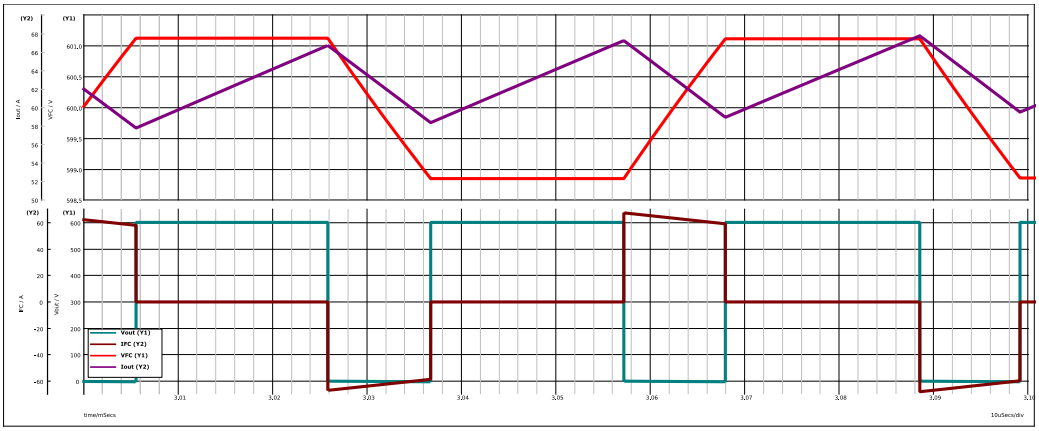

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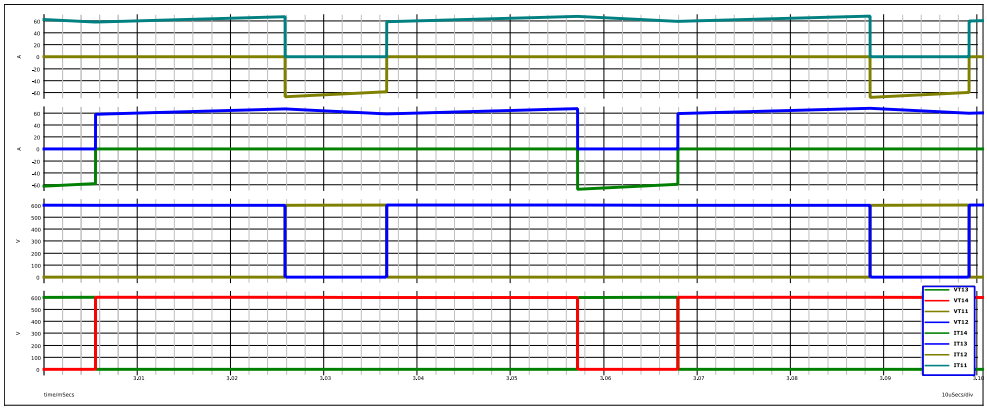

Figure 5: The typical curves:

a) the gate signals

b) the output and the flying capacitor voltage and current

c) the voltage and the current of the semiconductor

As it is shown in Figure 5 *b)* the flying capacitor voltage is changing during the two neutral states. If this two states are asymmetrical, one of the state will be longer, resulting in a net increase or decrease of charge in the capacitor. The voltage of the flying capacitor will increase

or decrease. To balance the voltage of the flying capacitor the average current of the capacitor have to be zero.

In Figure 6 the flying capacitor voltage, the output voltage and current, and in Figure 7 the output current and voltage can be seen, measured on the evaluation board of Vincotech. For the measurements the offset balancing method was used which will be explained later.

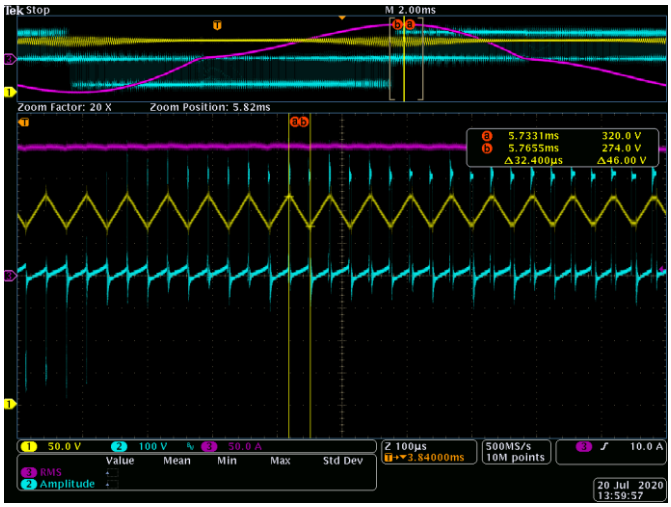

Figure 6: The voltage of the flying capacitor (CH1), the output voltage (CH2) and the output current (CH3) in the EVA Board

Figure 7: The output voltage (CH2) and the output current (CH3) in the EVA Board

3 Design Challenges of Flying Capacitor

3.1 Sizing

The voltage supplied by the flying capacitor has a key role in this topology. To keep the voltage ripple of the capacitor low a suitable capacitor size is needed. To determine the minimum needed capacitance the switching frequency, the output current and the maximum allowed voltage ripple need to be considered. The size of the capacitance can be calculated as:

$$C_{FCmin} = \frac{I_{peak}}{\Delta V_{FC} \cdot p \cdot f_{SW}}$$

Where ΔU_{FC} is the maximum allowed voltage ripple, I_{peak} is the maximum current, p is the number of the commutation cells, and f_{SW} is the switching frequency of the transistors.

3.2 Startup

Before starting the inverter the voltage of the flying capacitor is zero. Before normal operation it has to be charged to the adequate voltage level. If the inverter would be started without a charged flying capacitor, the inner half-bridge would get full DC-link voltage. The capacitor would be charged instantaneously, resulting in a short circuit current on the outer switches and on the flying capacitor, while the inner switch and the flying capacitor would get over voltage. There are two ways to address the pre-charge challenge. One is the passive one, the other is the active pre-charge one.

In case of passive pre-charge a resistive voltage divider is used on the input of the inverter, which will set the flying capacitor voltage before starting. This can be seen in Figure 8. In this case a resistor is used in parallel with the flying capacitor (R_2) with the same resistance as the sum of resistors between DC+ FC+ (R_1), and FC- DC- (R_3). As the voltage divider will dissipate during the normal operation high resistance values have to be used. However, the startup time also depends on the resistance. So the higher the resistance, the longer the startup. The starting time can be calculated from the value of the resistors and the capacitor.

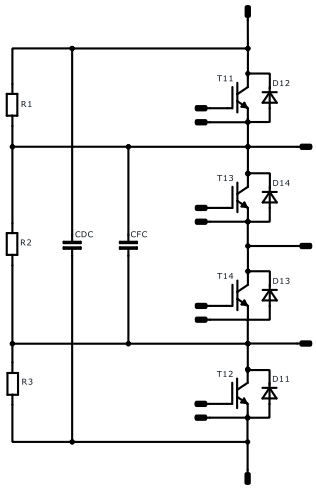

Figure 8 The passive pre-charge

It can be calculated with Kirchhoff's Current Law:

$$\frac{V_{DC} - v_{FC}(t)}{R_1 + R_3} - \frac{v_{FC}(t)}{R_2} = C * \frac{dv_{FC}(t)}{dt}$$

Given that:

$$R_1 + R_3 = R_2 = R$$

Resulting in:

$$\frac{V_{DC} - 2 * v_{FC}(t)}{R} = C * \frac{dv_{FC}(t)}{dt}$$

Concluding:

$$v_{FC}(t) = \frac{V_{DC}}{2} + c_1 * e^{-\frac{t}{\frac{R}{2}*C}}$$

The voltage is changing by an exponential function bearing to $\frac{V_{DC}}{2}$. As the voltage won't reach $\frac{V_{DC}}{2}$ the starting time has to be calculated until it will reach the regulation range (e.g., 90 % of $\frac{V_{DC}}{2}$). At $t = 0\ s$ the voltage of the capacitor is zero. Given that, c_1 can be calculated.

$$V_{FC} = 0;\ t = 0$$

$$0 = \frac{V_{DC}}{2} + c_1$$

Resulting in c_1 equal to $-\frac{V_{DC}}{2}$.

Finally:

$$v_{FC}(t) = \frac{V_{DC}}{2} - \frac{V_{DC}}{2} * e^{-\frac{t}{\frac{R}{2}*C}}$$

By this, the time constant is:

$$\tau_1 = \frac{R}{2} * C$$

The current and the voltage of the capacitor can be seen in Figure 9 a).

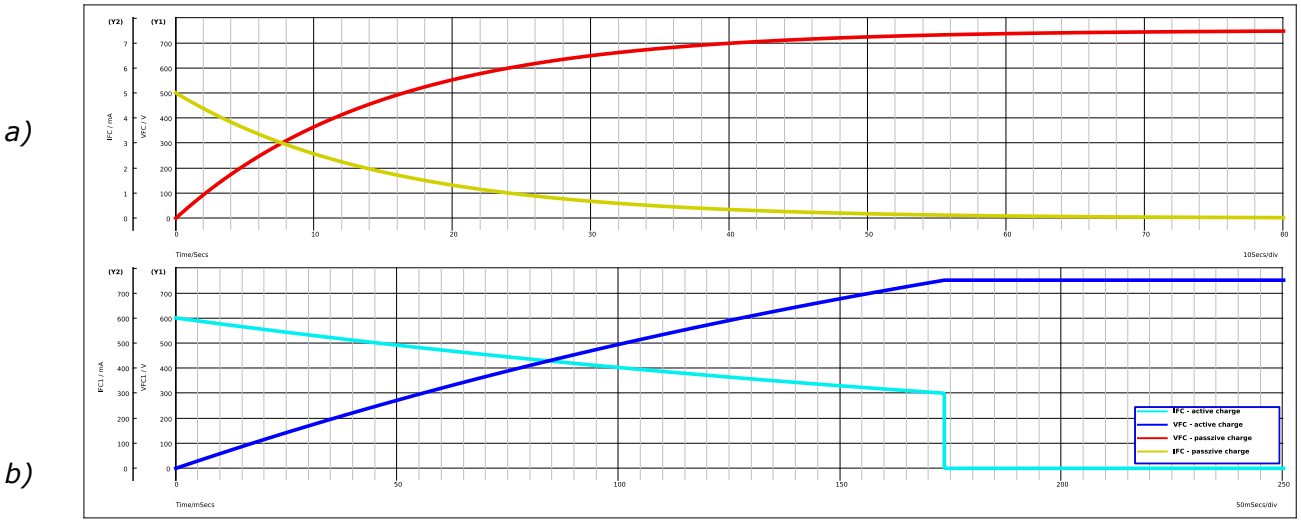

Figure 9: The voltage and the current of the flying capacitor during startup

a) in case of passive pre-charge

b) in case of active pre-charge

The other way is active charging. In this case, a resistor has to be added in series with the inverter for limiting the inrush current after the outer switches are switched on simultaneously. The DC-link voltage should be connected to the inverter. With this method the integrated DC-link capacitor won't be discharged. This can be seen in Figure 10. The capacitors will charge with τ_2 time constant.

Where:

$$\tau_2 = R * C$$

If an integrated DC-link capacitor is assembled in the power module, the charging resistor cannot be placed between the capacitor and the module. In this case:

$$C = C_{FC} + C_{DC}$$

When the flying capacitor reaches $\frac{V_{DC}}{2}$, the outer switches should be switched off immediately. So the flying capacitor won't be overcharged. After switching off the outer switches the integrated DC-link capacitor will be charged further.

The changing of the capacitor voltage can be calculated:

$$\frac{V_{DC} - v_{FC}(t)}{R} = C * \frac{dv_{FC}(t)}{dt}$$

$$v_{FC}(t) = V_{DC} + c_2 * e^{-\frac{t}{R*C}}$$

At $t = 0\,s, V_{FC} = 0\,V$. Resulting in:

$$v_{FC}(t) = V_{DC} - V_{DC} * e^{-\frac{t}{R*C}}$$

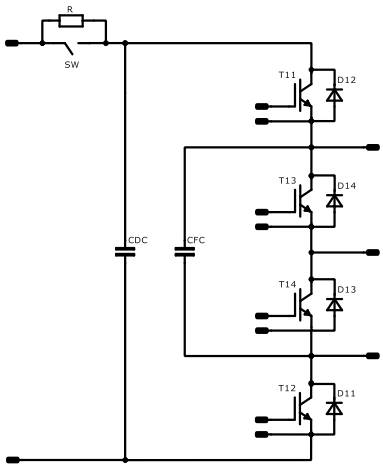

Figure 10: The active pre-charge

To reduce losses, another switch or relay should be used to eliminate the limiting resistance when the inverter has started. The operation of the active charging can be seen in Figure 9 b).

3.3 The Balancing of the Capacitor

Balancing the flying capacitor voltage is an important aspect of this topology. For the appropriate operation of the inverter the flying capacitor voltage has to be half of the input voltage. For the voltage regulation the voltage of the flying capacitor, the input voltage and the output current direction need to be considered. Those have to be measured in the inverter. As it was presented previously, the flying capacitor voltage during the neutral states can be charged or discharged (Table 1). There are two ways to approach.

The various modes can be considered as states which changing in a determined sequence. In normal operation the sequence is the following in the first half-period:

…Mode1→Mode2→Mode1→Mode3→Mode1…

In the second half-period it is:

…Mode4→Mode2→Mode4→Mode3→Mode4…

If the duration of one of the neutral states (Mode two or Mode three) changes, the flying capacitor voltage will change accordingly. As the output duty cycle should not change, the increase of one neutral state should be compensated by decreasing the other. It is also possible to use only one neutral state instead of two. As a result the change of the flying capacitor voltage will be faster.

…Mode1→Mode2→Mode1→Mode2→Mode1… or

…Mode1→Mode3→Mode1→Mode3→Mode1… in the first half-period.

The state diagram can be seen in Figure 11.

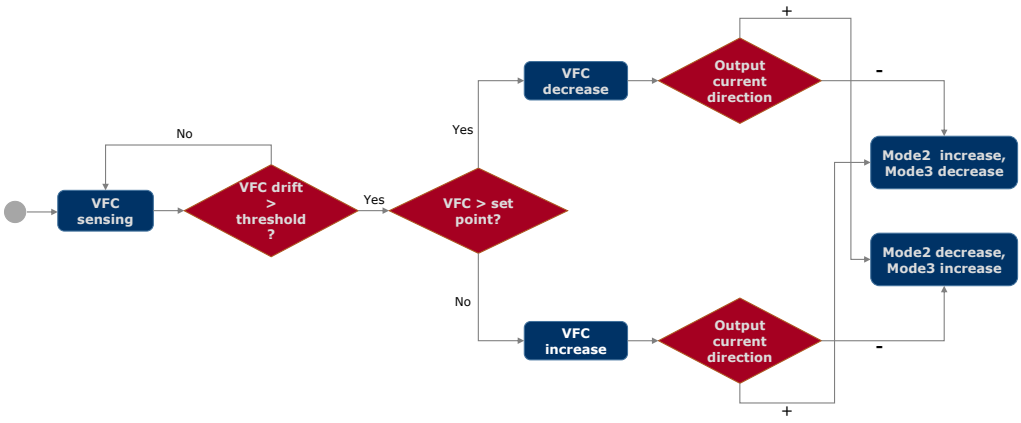

Figure 11: Voltage balancing state diagram

The control of the flying capacitor voltage can also be achieved by modifying the PWM signals. Here also the duration of the neutral states have to be modified. As a result the flying capacitor voltage changes. To change the duration an offset has to be added to one of the modulation signals. Then, one of the neutral states will be longer. To keep the same duty cycle on the output the inverse of the offset has to be added to the other modulation signal to shorten the other neutral state. In this way the output average voltage remains the same and the flying capacitor voltage will change. This can be seen in Figure 12.

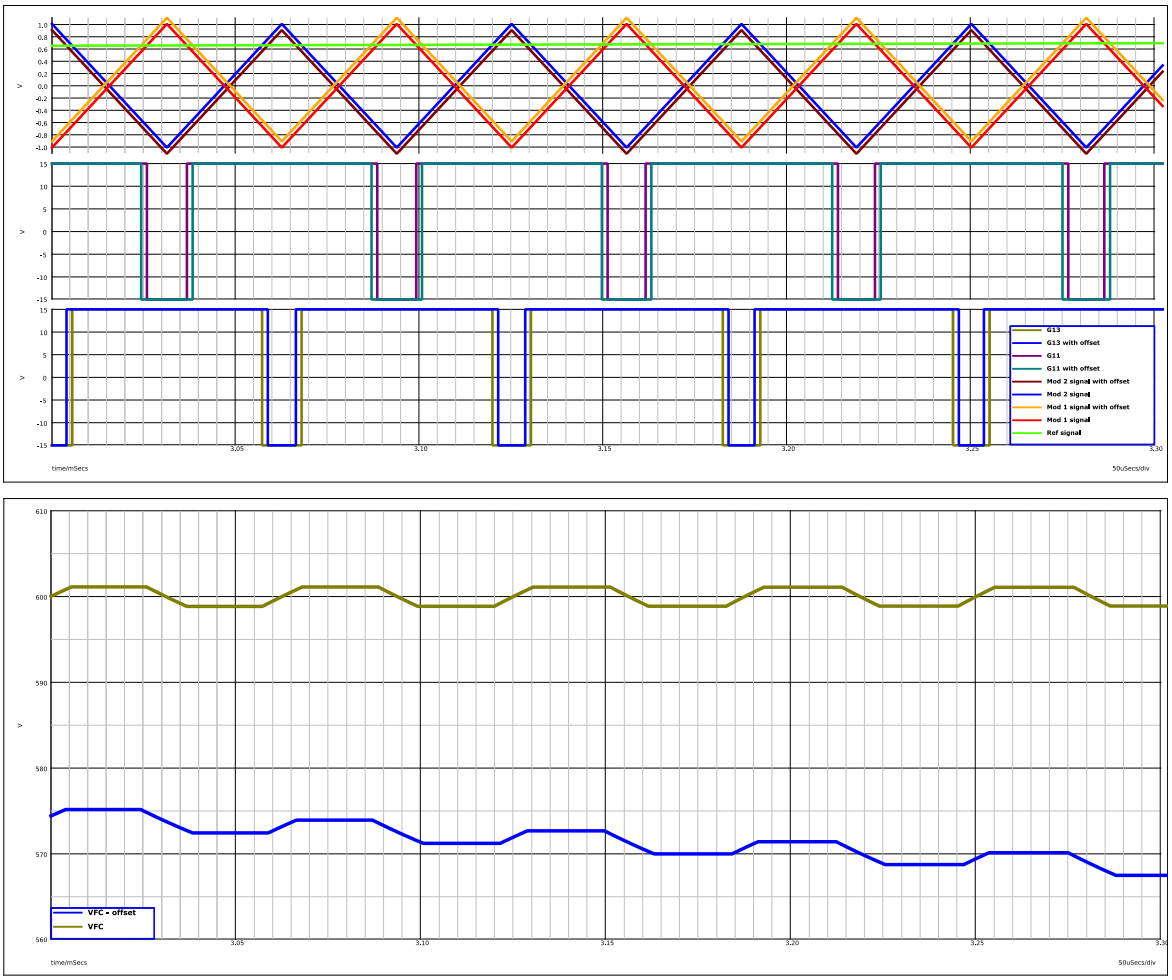

Figure 12: Changing the flaying capacitor voltage with offset

In both ways the action has to be chosen based on the capacitor voltage and the output current. So, if the current direction is changed, the action also have to be inverted (changing state or inverting the offsets) for the correct direction of the flying capacitor voltage changing.

4 Conclusion

The flying capacitor inverter is a highly efficient low cost solution for solar inverter applications. As the input is only two level in three phase application there is no need for enormous DC-link capacitors. However, the output is three level and the output frequency is a multiple of the switching frequency. The main advantages are the low capacitance needed on the input, the frequency multiplication, what is resulting in lower switching losses, smaller inductor or current ripple on the output and the lower EMI emission. The lower switched voltage enables higher

system voltage with the same components or the components voltage rating can be reduced, also leading to lower switching losses. The challenges of startup and the flying capacitor voltage balancing can be addressed easily. The above mentioned facts reduce the inverter costs and increase the lifetime of the inverter as compared to traditional topologies and the flying capacitor inverter became a strong alternative to them.