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3-PHASE PFC TOPOLOGY USING CONSTANT POWER CONTROL

HOW TO GET HIGHER POWER DENSITY AND COST SAVINGS IN PASSIVES

PCIM Europe Conference 2022

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Highly Efficient PFC Topology Using Constant Power Control Enabling Higher Power Density and Cost Savings in Passives

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The Power Point Presentation will be available after the conference.

Abstract

Higher system efficiency in motion control applications can be achieved by increased use of SiC components. They enable increased switching frequencies and smaller magnetics, but with higher semiconductor costs in power modules. The Current Synthesizing PFC (CSPFC) topology, a type of Power Sink/Source Inverter (PSI), can help reduce the SiC component costs while achieving 99% PFC efficiency. This paper presents results from an experimental hardware prototype, demonstrates the advantages of the topology and explores further theoretical improvements of the Total Harmonic Distortion (THD) through the DC-link capacitor current compensation.

1 Introduction

In response to the growing demand for higher integration, increased complexity and greater efficiency in embedded drive systems, e.g. for air-conditioning and compressor-based heating systems, new topologies which lead to cost-effective solutions with the highest power density and best efficiency are required.

Compared to the state of the art topologies such as the 3-level Neutral Boost PFC converter, the Current Synthesizing PFC (CSPFC) topology requires no line inductors, no large DC-link capacitors for energy storage and fewer fast switching semiconductors - only two SiC MOSFETs in Half-Bridge compared to the six fast switching IGBTs and SiC diodes to achieve the similar efficiency.

To illustrate the advantages of the CSPFC topology, an experimental hardware prototype was developed.

2 Three Phase CSPFC Converter

The CSPFC topology is a type of Power Sink / Source Inverter (PSI), represented in Fig. 1. The concept, which was first introduced in [1], is based on two laws of physics: *Kirchhoff´s Law*, where the sum of currents of the 3-phase AC is equal to zero at any moment,

$$i_R + i_S + i_T = 0 \quad (1)$$

and the *Law of Energy Conservation*, where, in power converters with no significant energy storage, the energy entering or leaving the 3-phase AC side is equal to the energy leaving or entering the DC side.

The above schematic is given for the unidirectional PFC converter. It consists of a three-phase bridge rectifier, an IGBT multiplexer (MUX) for the bidirectional switching, and a current injecting circuit, which is represented by two SiC-MOSFETs in half-bridge configuration and an inductor.

The u_{dc+} is following the highest voltage of three phases and the u_{dc-} respectively the lowest voltage.

$$u_{dc+} = \max(u_R, u_S, u_T) \quad (2)$$

$$u_{dc-} = \min(u_R, u_S, u_T) \quad (3)$$

The MUX IGBTs, which are connected to the ac mains, are selecting the “middle” phase and injecting the 3rd harmonic current through the half-bridge switches and L_{inj} inductor. The bidirectional switches are conducting 1/3 of the sinusoidal cycle. The high frequency switching is performed only by current synthesizing Half-Bridge, which is

switching only the low value of 3rd injecting current.

In a symmetrical 3-phase network, where the power is constant during the sinusoidal period, it is sufficient to control the current in one of the input phases at a time. The other two phase´s currents will follow for a symmetric load.

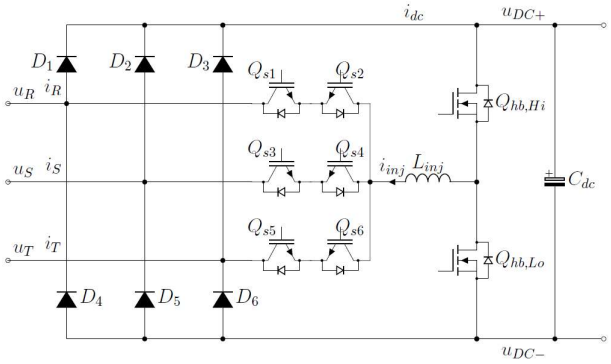


Fig. 1 Schematic of unidirectional three-phase CSPFC converter topology

The basic curves of the CSPFC topology based on the simulation are shown in Fig. 2:

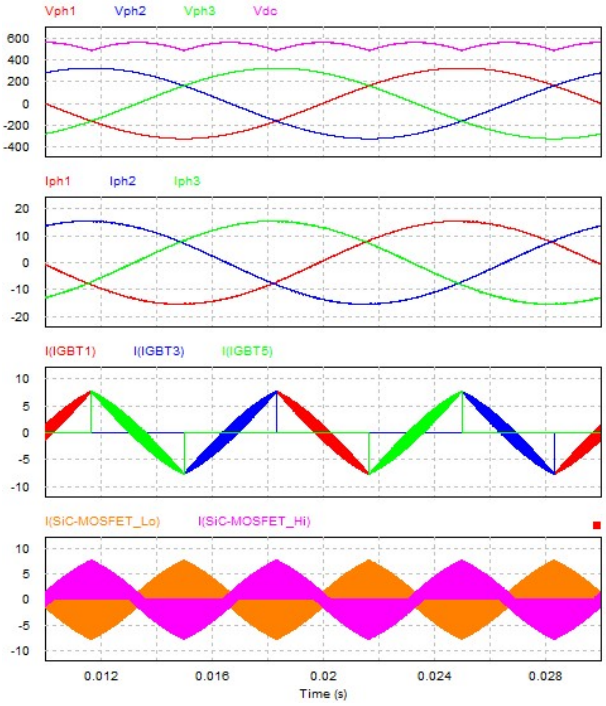
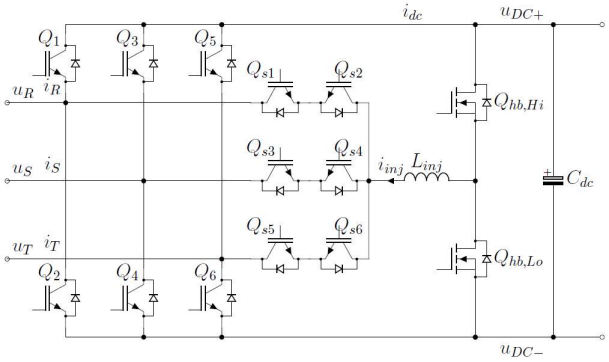


Fig. 2 Basic curves of 3-phase CSPFC topology: the ac input voltage and dc-link voltage; the ac input current; the current in the MUX IGBTs and current injected in the Half-Bridge.

This topology is also suitable for the bidirectional PFC converters, in this case the rectifiers could be easily replaced by the IGBTs as shown in Fig. 3.

Fig. 3 Schematic of bidirectional three-phase CSPFC converter topology



3 Hardware Prototype of 11 kW Three-Phase CSPFC for Motion Control Application

The Fig. 4 shows an experimental hardware prototype. It consists of three parts: a CSPFC converter, a booster converter and a 3-phase sixpack inverter. This allows operation of CSPFC converter in two different modes.

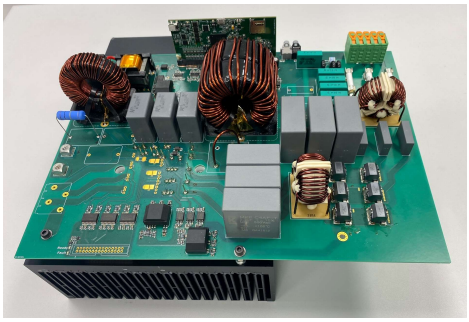


Fig. 4 Picture of CSPFC hardware prototype

In the first solution, shown in Fig. 5, a booster stage is added following the CSPFC converter in order to assure constant power mode and regulate dc-link for constant voltage and so getting independence from actual load conditions on the dc-link. Because of the additional booster stage, this solution has higher losses, but the advantage is that the output voltage can be boosted to any constant voltage level.

In Fig. 6, there is no booster stage, thus improving the system efficiency significantly, because the sixpack has lower losses due to the lo wer switching frequency and lower current. However, the six pack has to deal with the 300 Hz voltage ripple which will be present on the C_{dc} capacitor through the three-phase rectifier.

This circuit requires that the load in this case, e.g. sixpack motor inverter, is controlled for constant power in time. Additionally, the value of DC link capacitor cannot be any high, because the 300 Hz voltage ripple on the rectifier output will result in charge / discharge current through the capacitor. This charge / discharge current will unbalance the constant input power and thus result in distortion on the input.

The distortion caused by the 300Hz current in dc-link capacitor can be compensated theoretically by supplying a reactive THD compensation current. This is described in chapter 4.

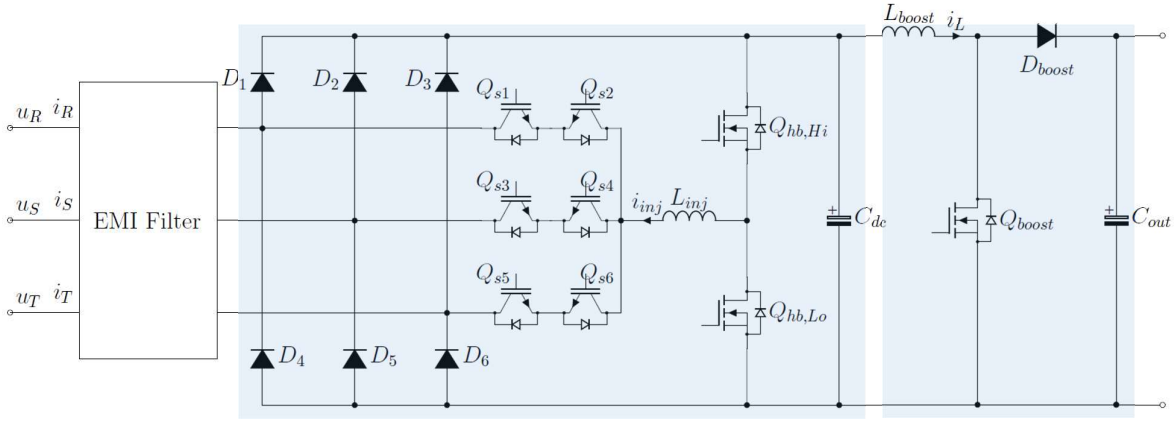


Fig. 5 Schematic of CSPFC converter with a booster stage

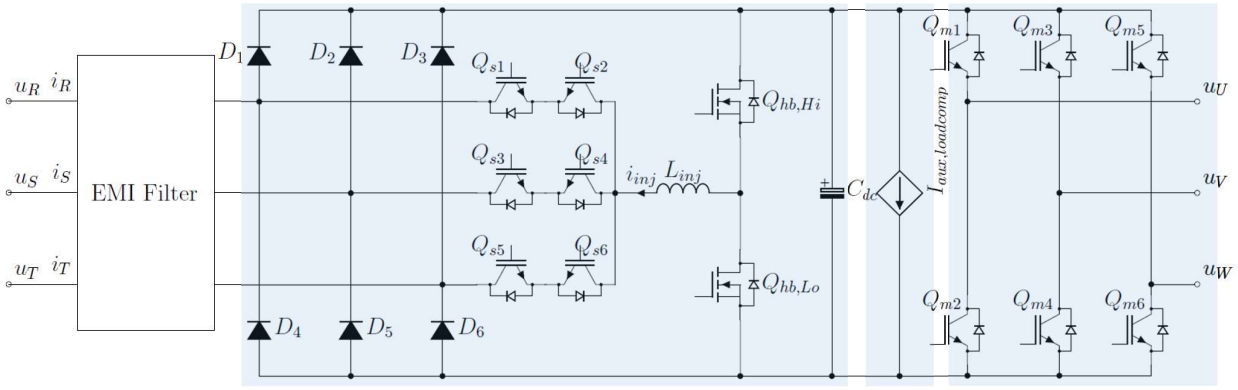


Fig. 6 Schematic of CSPFC converter with 3-phase sixpack inverter

3.1 Measurement Results

The experimental measurements of CSPFC converter with booster stage was performed. The operating conditions are given in the table below.

Parameters	Values
Input voltage (Line-to-Neutral)	$U_{NL} = 230\ V_{rms}$
Line Frequency	$f_L = 50\ Hz$
Switching Frequency of Half-Bridge	$f_{sw} = 100\ kHz$
Switching Frequency of Booster	$f_{sw} = 100\ kHz$
Nominal Booster Output Voltage	$U_{dc} = 700\ V$
Nominal Output Power	$P_{nom} = 11\ kW$

Table 1: Operating conditions for the CSPFC converter with a booster stage

Component	Description
$Q_{hb,Lo\text{-}Hi}$	SiC MOSFET – 1200 V, 75 mΩ
$Q_{s1\text{-}6}$	IGBT & FWD – 1200 V, 10 A
$D_{1\text{-}6}$	Rectifier – 1600 V, 28 A
Q_{boost}	SiC MOSFET – 1200 V, 32 mΩ
D_{boost}	SiC Diode – 1200 V, 15 A
L_{boost}	Sendust toroidal core 2x RS250060 290 µH
L_{inj}	Sendust toroidal core RS226060 390 µH
C_{dc}	1 µF, 650 V
C_{out}	2 µF, 1000 V

Table 2: List of used semiconductors and main passive components

Table 2 is also giving an overview about the used main components:

3.1.1 AC Input Current

Fig. 7 shows the measured AC input current at nominal load and input voltage. Sinusoidal input currents with minimal distortion can be observed. The power factor above 0.99 can be easily achieved.

The measurement results at very low partial load, i.e. 10% of nominal power is given in the Fig. 8. There the THD exceeds 5% and the PF decreases to 0.88, because of the EMI filter's effect.

The measured total harmonic distortion of the input current as a function of output power is shown in Fig. 9.

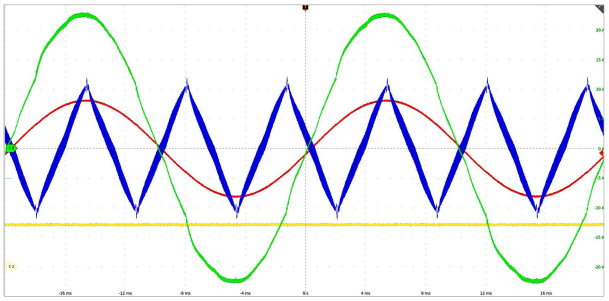


Fig. 7 Measurement results CSPFC operating at nominal power - ac input current (green), injected 3rd harmonic current in inductor (blue), input voltage (red) and output voltage (yellow) at P = 11 kW, U_1 = 230 V_{rms} and U_{out} = 700 V_{dc}.

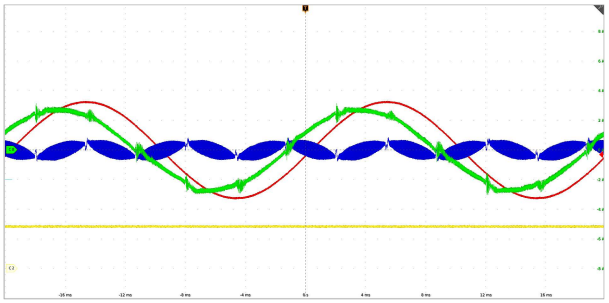


Fig. 8 Measurement results when CSPFC operating at 10% of nominal power - ac input current (green), injected 3rd harmonic current in inductor (blue), input voltage (red) and output voltage (yellow) at output power of P = 1.1 kW, U_1 = 230 V_{rms} and U_{out} = 700 V_{dc}.

3.1.2 Efficiency

The efficiency measurement was performed for the CSPFC and booster stage. The system efficiency of 98.1% could be achieved at the full power of 11 kW.

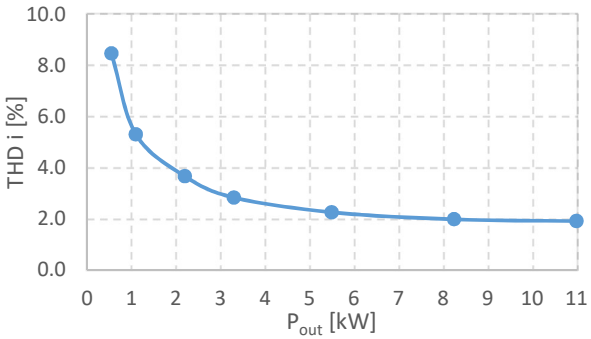


Fig. 9 Total harmonic distortion (THD) values of the ac input currents as a function of output power for nominal input and output voltages. Measured using an ITECH IT7900 Regenerative Grid Simulator.

The detailed distribution of the calculated component losses is given in Fig. 10. The semiconductor power losses are calculated based on Vincotech´s real characteristic data.

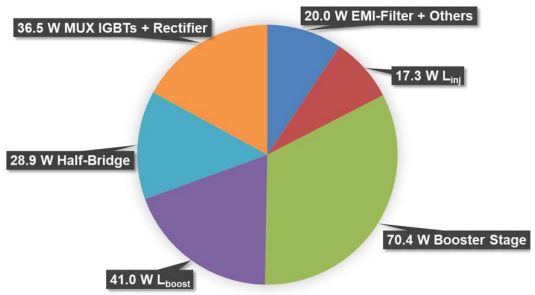


Fig. 10 The distribution of power losses at the nominal operating conditions for CSPFC converter with booster stage.

Taking into account high power losses of the booster circuit and deducting it from total system losses, the efficiency of 99.1 % for CSPFC converter at nominal load of 11 kW can be achieved.

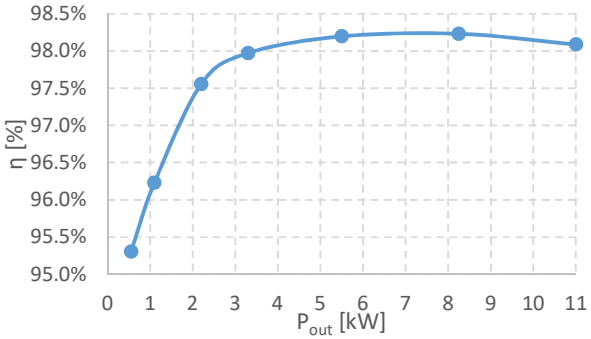


Fig. 11 The calculated system efficiency using an ITECH IT7900 regenerative grid Simulator and a DC load.

4 300 Hz DC-Link Capacitor THD Compensator

The reactive current compensation has been integrated into auxiliary circuit. An external board represented in Fig. 12 with high ohmic half-bridge, consisting of two 1200 V 350 mΩ SiC MOSFETs was designed. Its functional schematic is shown in Fig. 13.

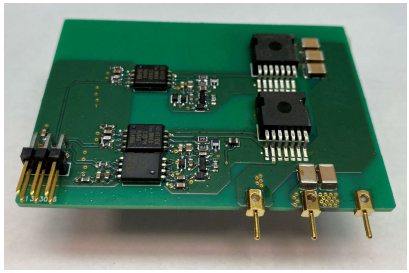


Fig. 12 THD-compensator board

The board can be connected in parallel to the rectifier output and capacitor C_{dc} as shown in the Fig. 6. The high ohmic half-bridge can be operated in ZVS mode with a switching frequency of 200 kHz and consuming only about 3 Watts.

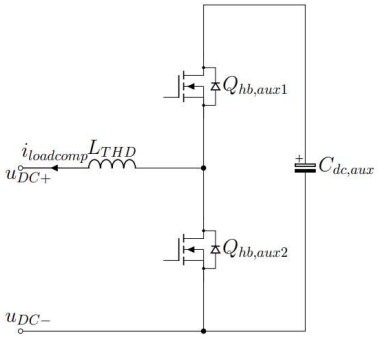


Fig. 13 Schematic of high-ohmic half-bridge for THD-compensator board

The simulation results in Fig. 14 and Fig. 15 show the input current quality without and respectively with THD compensator board.

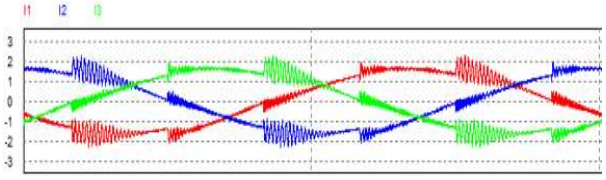


Fig. 14 The simulated results of CSPFC converter with sixpack inverter showing input current with THD of 13% at P_{nom} =10%

The additional advantage of the 300 Hz dc-link capacitor compensation method is that EMI input filter can be further reduced and the efficiency of the PFC stage increased to 99,3%.

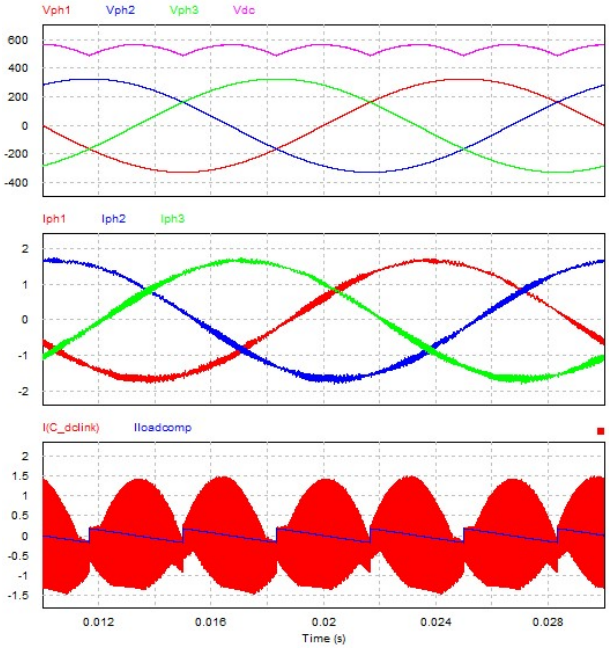


Fig. 14 The simulated results of DC-link capacitor current compensation showing THD of 3.3% at P_{nom}=10%: the ac input voltage and dc-link voltage; the ac input current; the dc-link capacitor current and THD compensation current sawtooth

5 Conclusion and Outlook

A functional hardware prototype was developed to investigate the benefits of CSPFC topology for the unidirectional PFC application. A very high efficiency of 99.1% at a switching frequency of 100 kHz has been achieved, and the IEC standard requirements for total harmonic distortion and power factor easily met.

Furthermore, through the implementation of the dc-link capacitor current compensation, the THD can be decreased below 5% even at 10% of the nominal load.

The CSPFC topology enables cost reductions for SiC components, weight and size savings in magnetic components, and elimination of the line inductors. The high frequency choke injects about the half of the amplitude phase current [2]. In addition, the elimination of large electrolytic DC-link capacitors for the energy storage brings valuable benefits by increasing life time of the electronics.

The highly efficient CSPFC topology is suitable for

various applications such as motion control, EV-chargers and renewable energy. It enables cost-optimized system design with increased switching frequency, high power density and low losses.

As an outlook of the project, the measurements of CSPFC converter with sixpack inverter is planned. In this operating mode of CSPFC, the benefits of THD compensator circuit will be verified due to real measurements as well.

6 Reference

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