The Challenges of Using SiC MOSFET-based Power Modules for Solar Inverters

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Abstract

This paper examines SiC MOSFETs as a viable option for meeting the rising demand for faster switching and greater efficiency in 1500 V solar applications. It looks at their benefits – SiC MOSFETs enable deeper integration and greater power density – and their drawbacks in terms of switching performance in power module applications. The intrinsic properties of the latest generations of devices appear to inhibit performance and reliability. This paper analyzes the root cause of these limitations and proposes solutions to overcome them.

1. Electrical performance

1.1. Advanced Neutral Point Clamped (ANPC) Solar Inverter

The object of investigation is an ANPC (active neutral point clamped) power module equipped with Si IGBTs and SiC MOSETs as bare die. This ANPC is an improved version of the three-level NPC inverter topology. Figure 1 depicts an ANPC schematic with four grid-frequency synchronized IGBTs (T1-T4), their anti-parallel diodes (D1-D4), and two fast-switching MOSFETs (T5 and T6). The target application is a 1500 V string inverter with high switching frequency (up to 64 kHz) and high efficiency. Figure 1 shows one phase out of the three-phase inverter system, including the power module, dc-link capacitors (C_{DC1} and C_{DC2}) and inverter choke (L_{AC}).

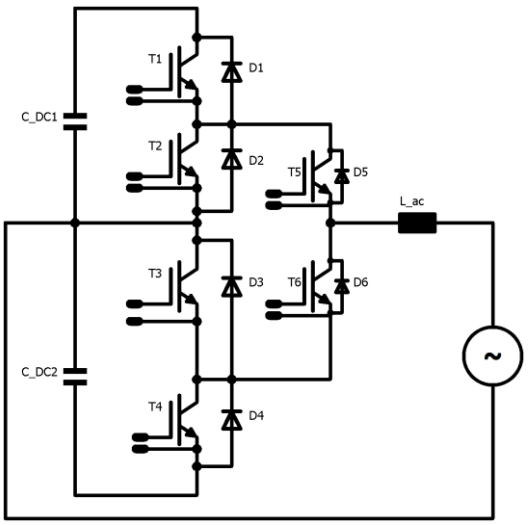

Fig 1. Active neutral point clamped (ANPC)

The switching performance of various suppliers' SiC MOSFETs was investigated in a hard-switching, totem-pole half-bridge configuration. All measurements were taken at a double-pulse characterization test station with a power module as shown in figure 1. The same DCB layout was used for all three measurements to ensure the parasitic inductance attributable to the layout, wire bonding and distance between pins would not affect the results. The only variable was the investigated type of SiC MOSFET. This characterization test station's low-inductive drive circuit supports positive and negative multiple-ampere gate drive currents. One SiC MOSFET was selected as an example for the in-depth investigation conducted for this paper.

The double-pulse measurement assessed the low-side MOSFET T6's switching waveform and switching energies. This MOSFET formed a commutation pair with the body-diode of the high-side MOSFET T5. T6 stayed on for a prolonged

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period to build up current, and was then switched off for a short time to allow the current to commutate fully in the body-diode of the opposite MOSFET T5. Then the low-side MOSFET T6 was turned on again and the MOSFET and diode's switching waveforms and energies were measured at that moment.

1.2. Double-pulse measurement result

The turn-on waveform of the low-side MOSFET T6 shown in figure 2 indicates a sharp spike of the drain current followed by ringing of the drain current and gate voltage. This indicates a parasitic turn-on of the opposite device, also called cross-conduction or shoot-through.

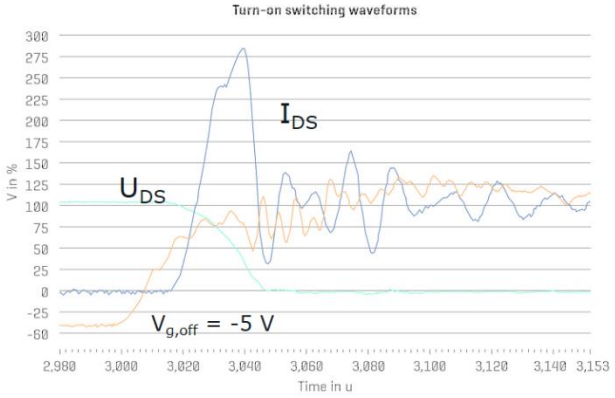

Fig. 2. Cross-conduction at low-side SiC MOSFET turn-on, U_{ds}: light blue, I_{ds}: dark blue, U_{gs}: yellow (U_{dc}=600 V, I_{ds}=140 A, T_j=150 C, V_g=-5/16 V)

1.3. Explanation of the root cause

Before the low-side MOSFET T6 turns on, the current is freewheeling in the body diode of the high-side MOSFET T5. During turn-on, the current commutates from the high-side diode to the low-side channel (figure 3). This causes the diode to block and the voltage potential of the midpoint to change with high dv/dt from DC+ to 0 V.

Figure 4 shows the position of the SiC MOSFET's intrinsic capacitances. The Miller capacitance C_{gd} is located between drain and gate, while C_{gs} is between the gate and source, and C_{ds} is between the drain and source.

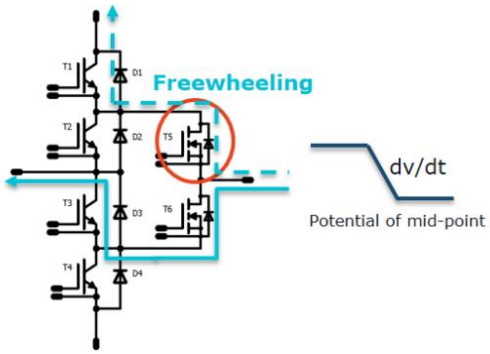

Fig. 3. The current path in hard-switched ANPC

The voltage across C_{ds} increases with high dv/dt. The current then flows through C_{gd} and C_{gs}. The voltage on C_{gs} rises. If it reaches the turn-on threshold, the MOSFET starts conducting current in its channel.

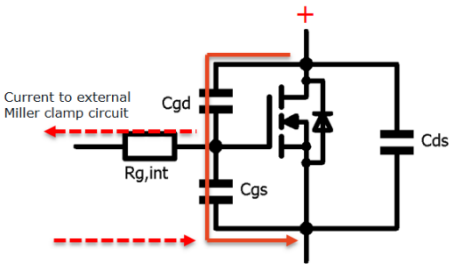

Fig. 4. The SiC MOSFET's internal device capacitances and gate resistance

This renewed turn-on causes the current spike in the low-side MOSFET's drain shown in figure 2, and therefore also high switching energies. The operation junction temperature limits the highest acceptable power dissipation per MOSFET, which means the high switching energy limits the maximum switching frequency.

2. Proposed solutions

This chapter describes potential solutions, analyzes their effectiveness and looks at how these are put into practice.

2.1 Miller clamp circuit

A common way of removing the injected current from the device is to install an external Miller clamp circuit in the gate driver. The external clamp circuit's effectiveness depends on the

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inductance between the clamp circuit and the MOSFET, and on the internal gate resistance.

The gate loop's inductance is below 4nH, including the module's pin, bond wires and DCB copper tracks.

In this case, the MOSFET's internal gate resistor limits effectiveness—the higher the gate resistor value, the less effective the external Miller clamp circuit. The gate resistor in this example has several ohms, which prevents the charge's removal.

2.2. Negative gate voltage bias

Another option is to increase the negative gate voltage bias until any parasitic turn-on is undetectable. However, most suppliers limit the maximum negative gate voltage to a value of around -5 V, including all transients. Experiments show that a negative voltage spike appears when the MOSFET is turning off. This spike imposes a limit on the static negative gate voltage as the sum of both may not exceed the maximum ratings. In that case, this solution is not an option.

If the negative spike exceeds the given limits for device reliability, this will cause the gate oxide to degrade. This has a negative impact on long-term reliability because the threshold voltage may decrease to zero as the oxide deteriorates.

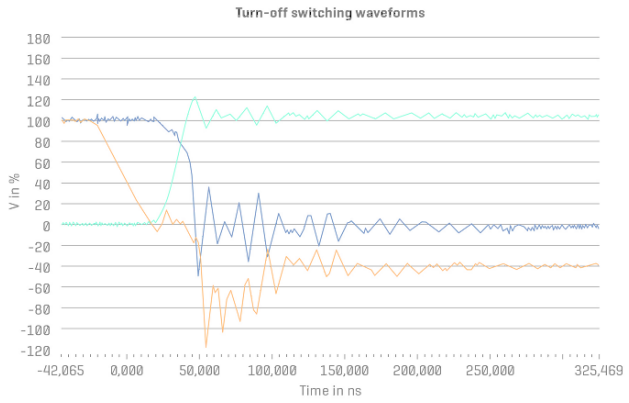

Fig. 5. Low-side SiC MOSFET turn-off, U_{ds}: light blue, I_{ds}: dark blue, U_{gs}: yellow (U_{dc}=600 V, I_{ds}=140 A, T_j=150 C, V_g=-6/16 V)

2.3. ANPC with split output

Another proposed solution is to decouple the high- and low-side MOSFETs by splitting the circuit into two parts with a separation inductance in between.
The module's pin stray inductance serves as the separation inductance. No additional external circuit components are necessary.
Two additional diodes have to be added in the power module to keep the circuit functional (figure 6).

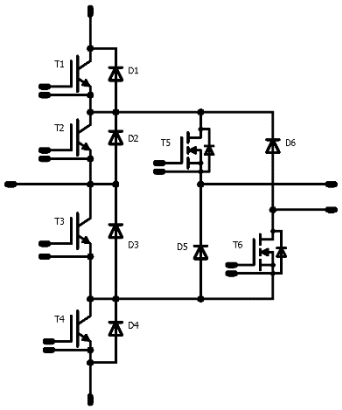

Fig. 6. ANPC with split output

The added inductance disables the given switch's output capacitance, thereby preventing exposure to high dv/dt and Miller capacitance-induced charging injected into the gate. This first step can reduce the second current spike (figure 7), but not eliminate it all together.

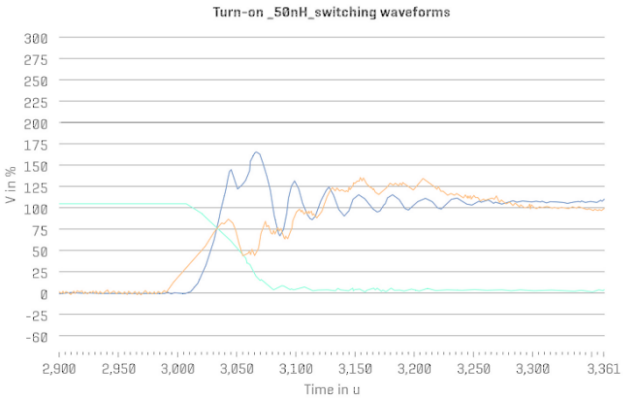

Fig. 7. Low-side SiC MOSFET turn-on with 50 nH separation inductance, U_{ds}: light blue, I_{ds}: dark blue, U_{gs}: yellow (U_{dc}=600 V, I_{ds}=140 A, T_j=150 C, V_g=0/16 V)

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2.4. ANPC with split-output and integrated gate capacitor

A further step can be taken to fully overcome the limitations imposed by the Miller effect: Install a capacitor in the module between the MOSFET's gate and source (figure 8). The absence of a second current spike in figure 9 shows that this prevents parasitic turn-on.
The gate capacitor reduces dv/dt, which has the added benefit of reducing EMC.

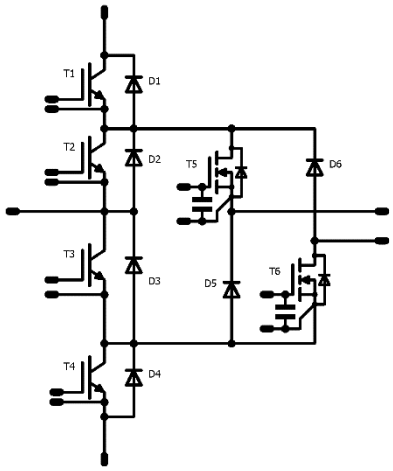

Fig. 8. ANPC with split output and gate capacitor

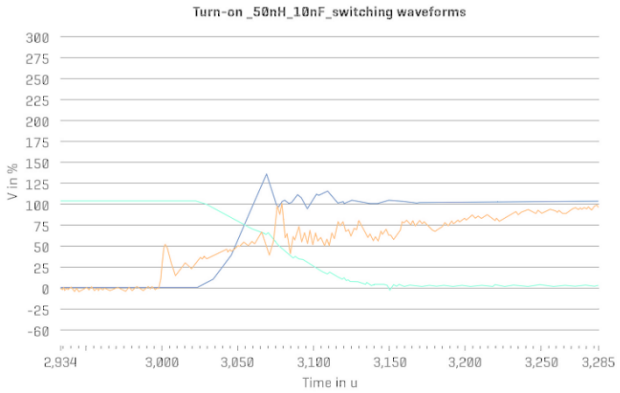

Fig. 9. Low-side SiC MOSFET turn-on with 50 nH separation inductance and 10 nF gate capacitor, U_{ds}: light blue, I_{ds}: dark blue, U_{gs}: yellow (U_{dc}=600 V, I_{ds}=140 A, T_j=150 C, V_g=0/16 V)

2.5. Smart gate driver

A smart gate drive may be used to dynamically drain the gate voltage to a more negative value when the Miller charge surges into the gate. Timing is essential here. The gate voltage has to be stepped down to a more negative value and back up to the nominal value after the high dv/dt crosses the half-bridge's midpoint.

The negative gate voltage spike shown in figure 5 can be used as the negative gate bias. This is done by turning on the opposite MOSFET at the moment the gate voltage is at its most negative value. The voltage added to the gate by the Miller effect increases the resulting voltage on the gate, but the absolute value will not reach the turn-on threshold (figure 10). The high-side gate voltage in this example was measured with a differential probe, which is why the capacitive current generated during low-side switching interfered with the measurement as can be seen here.

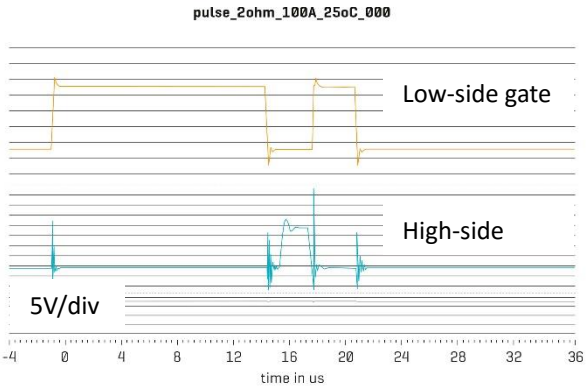

Fig. 10. A smart gate driver's low- and high-side gate timing

The smart gate drive may thus be a practicable solution. However, the timing has yet to be optimized and the solution's long-term reliability and effectiveness remains to be proven.

Conclusion

The above paragraphs describe and discuss various remedies to the root cause of the limitations of SiC MOSFETs operated in hard-switched, totem-pole applications. A SiC MOSFET has to operate reliably throughout its service life, so the main concerns to be taken into account here are the gate oxide and therefore the maximum positive and negative gate voltages. Exceeding the maximum device ratings in static or dynamic conditions may cause the gate structure to degrade and the threshold voltage to drift. This would eventually result in component

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failure and, as a consequence, device failure. A split output paired with an integrated capacitor between the gate and source as presented here can help overcome the limitations in switching performance and enable the device to be operated to its specifications.

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