SiC MOSFET-based Power Modules Utilizing Split Output Topology for Superior Dynamic Behavior

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1. Abstract

The body diode reverse recovery charge of a SiC MOSFET is lower than that of an Si MOSFET, but still not as beneficial as with SiC Schottky diodes. As the switching performance demands for new wide band-gap components increases, so do the requirements for the commutation process. The split output topology provides an additional tool to reduce turn-on losses and boost cross-conduction suppression.

2. The standard half-bridge topology's limitations

The standard half-bridge topology (see *Figure 1*) in power modules has its drawbacks for fast switching applications.

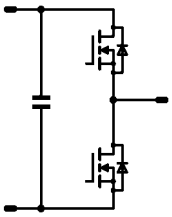

Figure 1: Half-bridge circuit with SiC-MOSFET

2.1. The body diode's reverse recovery current

If the body diode is used for freewheeling, the body diode's reverse recovery current increases switching losses (see *Figure 2*-1). The reverse recovery load (Q_{RR}) of SiC MOSFETs is far superior to that of Si MOSFETs. However, it is still significant for high frequency applications >50 kHz. The reverse current increases turn-on losses in the SiC MOSFET.

2.2. Output capacitance

The output capacitance of SiC-MOSFETs is relatively high. In a low inductive environment, the active MOSFET has to switch the capacitive load (see *Figure 2*-2) of the device, which is turned off. This increases turn on losses and EMI.

2.3. Cross conduction

SiC MOSFETs are designated for ultra fast switching, which causes high dV/dt at turn-on in half-bridge configurations. The voltage at the output changes from DC- to DC+ at turn-on of the high-side MOSFET. The parasitic capacitor between the drain and gate of the low-side MOSFET will induct a voltage (see *Figure 2*-3)

into the gate of the low-side MOSFET, which could trigger a parasitic turn-on. This will cause additional significant losses.

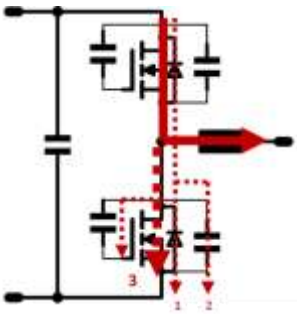

Figure 2: Parasitic action between the high-side and low-side MOSFET

3. Introducing the split output topology

The idea here is to separate the commutation circuit of the positive and negative half-wave or, in the case of a bidirectional DC-DC circuit, between the forward and backward conversion. The half-bridge is divided into one positive and one negative BUCK circuit (see *Figure 3*).

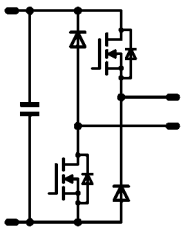

Figure 3: Half-bridge with split output topology

The commutation loop remains low inductive, whereas the low-side and high-side MOSFETs

are separated by the inductance of the external interconnection and optional inductance connected at the output. This inductance helps transcend the half-bridge circuit's limitations.

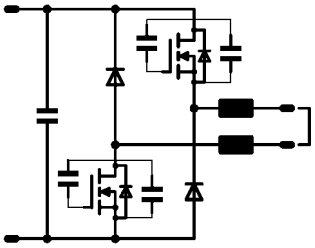

Figure 4: The split output interconnection's stray inductance severs the parasitic connection between the high-side and low-side MOSFET.

The split output allows the body diode with the additional SiC diode to be deactivated. In contrast to a configuration with an Si MOSFET, the voltage drop of the body diode in SiC MOSFETs is higher than in SiC diodes. The SiC diode takes the reverse current and prevents any reverse recovery charge in the body diode of the SiC-MOSFET. The inductance at the split output (*Figure 4*) decouples the high-side from the low-side MOSFET. In the case of a SiC MOSFET, the external interconnection's parasitic inductance already reduces the negative action of the output capacitance and cross conduction. At turn-on, the SiC MOSFET faces only the SiC diode with extreme low Q_{RR}. At turn-off, the commutation loop is closed with low induction via the SiC diode and the capacitor.

4. Synchronous rectification

In high-efficiency applications, the body diode's freewheeling efficiency improves with the MOSFET's synchronous turn-on in reverse direction, which reduces the voltage drop. This operating mode is feasible in a split output topology with very low or even just parasitic inductance at the output. This mode affords engineers the opportunity to reduce the size of the SiC diode to its pulse current limit. The output inductivity will delay the reverse conduction in the MOSFET by several ns.

5. SiC power module solutions with split output technology

The benefits of the split output have inspired a product definition that makes use of this design concept.

5.1. Module configuration with split output for 2-level operation

Three positive and negative BUCK circuits are combined in one module (see Figure 5) for universal use.

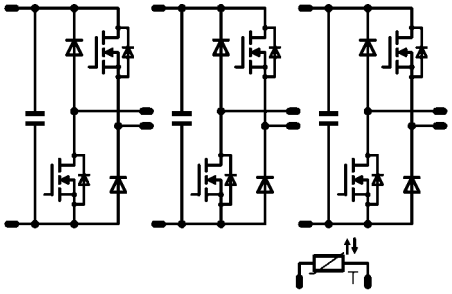

Figure 5: Module definition with a triple split output, half-bridge configuration and integrated DC-capacitors

The three circuits are not connected, which allows them to be used flexibly as individual circuits and to attach shunt resistors for current sensing. The integrated DC capacitor provides the low inductance required for the high turn-off speed of <10ns switches. This configuration may be used as a:

- ⇨ bidirectional DC/AC 3-phase inverter
- ⇨ or a 3-channel bidirectional DC-DC.

The successful *flow* 0 housing (see *Figure 6*) with Press-fit interconnection was chosen for this circuit's packaging.

Figure 6: Vincotech flow 0-package with Press-fit interconnection

5.2. Module configuration with split output for 3-level operation

Switches with split outputs may also be separated in mixed voltage NPC (MNPC) topologies (see *Figure 7*). In this case, the commutation loops are sited between the DC voltages and the neutral conductor. All connections between components in the commutation loop are low inductive, although the external interconnection's inductance is used between the high side and low side.

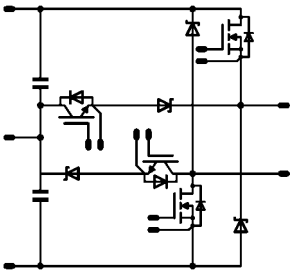

*Figure 7: The flow*MNPC 0-SiC *module's circuit with a split output*

A phase leg is integrated into a *flow* 0 package as pictured here.

5.3. Performance and efficiency

The split output topology transcends all the limitations of a SiC MOSFET. The efficiency calculated from the measured switching characteristics (see *Figure 8*) confirms that the tested SiC MOSFET is able to outperform the SiC JFET.

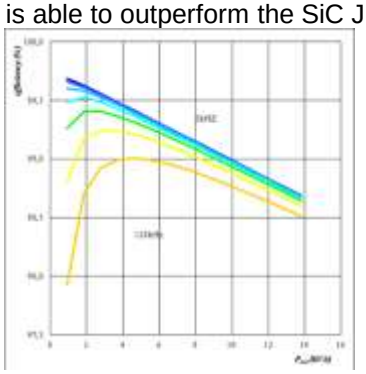

Figure 8: Efficiency per phase of a three-level flowMNPC 0 SiC module with 53 mΩ SiC BUCK MOSFETs

The inverter efficiency in an MNPC topology will achieve >99% efficiency at f_{PWM} = 64 kHz. The maximum efficiency at 16 kHz is 99.5%.

6. Conclusion

The split output topology installed at the module level negates the limitations of the SiC MOSFET. The module behaves in inverter applications in the same way as in a boost circuit. This makes it possible to achieve better performance and efficiency than with a SiC JFET or SiC BJT – and enjoy the added advantage of MOSFET technology's simple gate drive circuit.