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New Power Module Structure for Efficiency Improvement in Fast Switching Power Applications (>50kHz, >1kW)

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Power applications are forced to work at higher frequencies. This is caused by the continuous demand for compact and lightweight solutions and higher frequency reduce the mechanic size of the passive components as transformers, inductors and capacitors. Conventional power sources use big and heavy transformers running at 50 or 60Hz. At any given power to be transformed, the volume of the transformer is indirect proportional to the switching frequency. This means if the switching frequency will be increased, the volume will be correspondingly smaller - for the same power. The new generation of Switched Mode Power Supplies (SMPS) are running at ca. 100kHz so that the weight and the volume of the transformer is reduced to a minimum of i.e. 5% of the conventional 50Hz solution. But with high switching frequency the challenge is to optimize the overall efficiency of the converter were the switching losses become a significant portion of the total losses in the system.

Abstract

Power applications with switching frequencies of 50kHz and above require to pay specific attention to the switching mode and component selection as well as the layout and its parasitic side effects.

Switching losses which are becoming the dominant portion of the power losses at higher frequencies can be reduced by either using higher performance components or by optimizing the matching of the used components and their arrangement to each other. While the first solution is introducing higher system cost, optimizing components matching and arrangement can provide similar or even better results at lower cost. Power integrated modules are able to offer these advantages over discrete solutions and provide higher switching speed at lower total losses.

The following paper is focusing on hard switching PFC applications, SMPS and welding inverters with zero-voltage switching used at frequencies above 50kHz and an electrical output power of more than 1kW; it provides a detailed comparison for different transistor types (MOSFET, IGBT), technologies (NPT-, PT) of different suppliers and the corresponding diodes. This comparison is shown in this paper both in theory and by actual measurements.

The paper introduces:

- The most commonly used switching modes and their critical system parameters.
- Comparison of the different semiconductor components available on the market and their specific advantages and disadvantages.
- Influence of the semiconductor parameters for the power loss for the different switching modes used in today's power applications
- Different examples for component pin outs and corresponding PCB layouts and their influence on the system performance for fast switching power applications.
- Guidance for effective interpretation of values given in power component data sheets

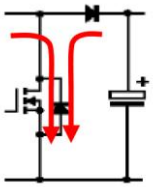
Background for the Loss Calculation:

The performance limitation for fast switching applications is in most cases the power dissipation caused by electrical losses in the semiconductors. That's why efficiency improvement is the most important target to achieve a cost effective design. With the calculation of the expected losses it is possible to compare the different solutions in advance without building them up on the bench.

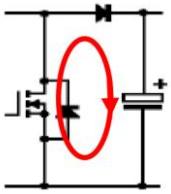
The losses in the semiconductors are:

- Static losses caused by the voltage drop in the semiconductor.
- Switching Losses are generated during switch on and switch off of the semiconductor. These losses are dependent on the switching mode and they are proportional to the switching frequency.

The static losses are defined by the current flowing through the semiconductor and by the semiconductor characteristics. The switching losses are also dependent on the switching mode. In hard switching applications, the diode will be commutated and the transistor must switch on additional the reverse recovery current of the free wheeling diode. The reverse recovery load of the diode (Qrr) influences the switch on losses of the transistor significantly. A fast diode is a must for high frequency and hard switching applications.

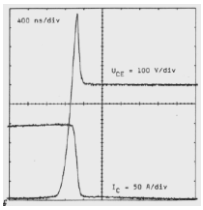


At switching-off the transistor the diode is commutated again and takes over the current.
But also here are special influences active. Due to parasitic inductance between the switch and the DC-capacitor additional losses will be generated.



The current change rate and the parasitic inductance cause a voltage spike at the transistor according to:

$$V_{CE}(peak) = V_{CC} + L \times di/dt$$



Theory - Switching Mode

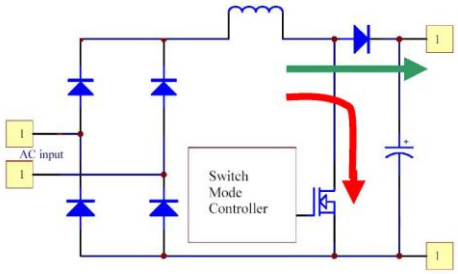
In high frequency power applications the switching conditions dependent on the topology and the switching mode. To determine the influence of the switching mode for the requirements of the semiconductors used following applications are investigated:

- Active power factor correction as a example for hard switching (HS)
- Welding Inverter as a representative application for zero voltage switching (ZVS)

The main difference in the loss calculation is the commutation of diode in hard switching applications. This influences the switch on losses of the switching component.

Active Power Factor Correction in Continuous Mode

The PFC-boost circuit which will be looked at in the following is a typical example for a hard switching application.



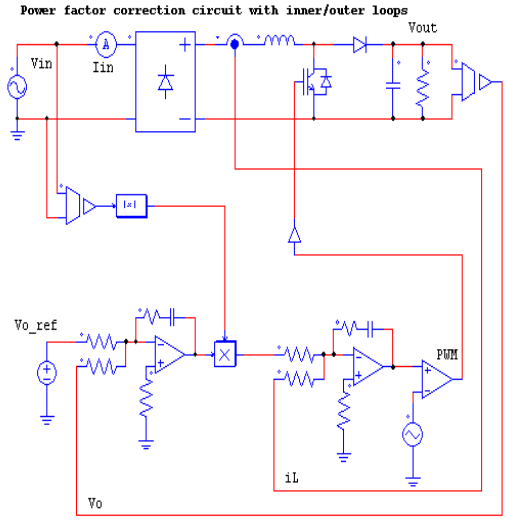
Function:
When the transistor is switched on energy is stored in the choke. After switching OFF the energy will flow via the diode into the capacitor. With an appropriate sequence of pulses at the transistor control input current is pumped during the complete half wave into the capacitor. With this boost topology an almost sinusoidal current sourcing is achievable.

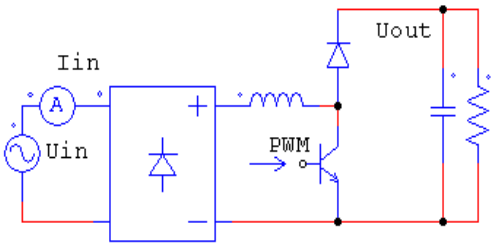
Here the simplified conditions for the loss calculation in a PFC application:

- Hard switching environment
- Static load
- Stable Vout DC voltage
- Fixed input frequency operation (50Hz)
- Modulation frequency >> input frequency

- Undistorted sinusoidal input voltage waveform
- Undistorted sinusoidal input current waveform
- Unity power factor
- Dead-time neglected

Model and equations for calculation:





Calculation of Losses

Following is the theory for the simplified loss calculation.
For simplicity input waveforms are full periodic sinusoidal signals:

$$Uin(t) = Uinpk * \sin(\omega * t)$$

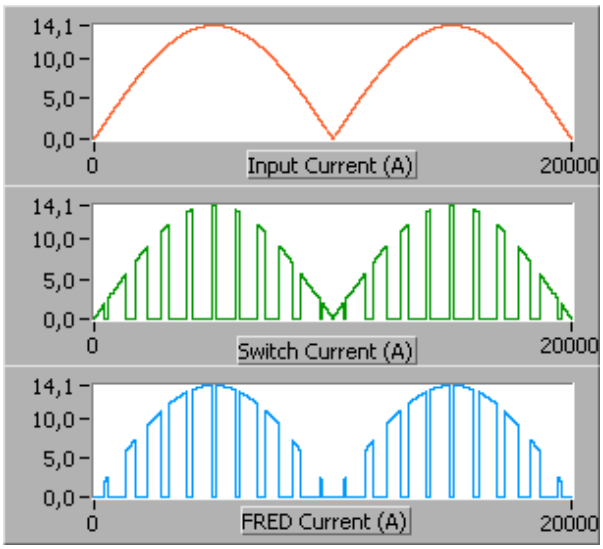
The first half wave (T/2) current for the controlled and uncontrolled switch:

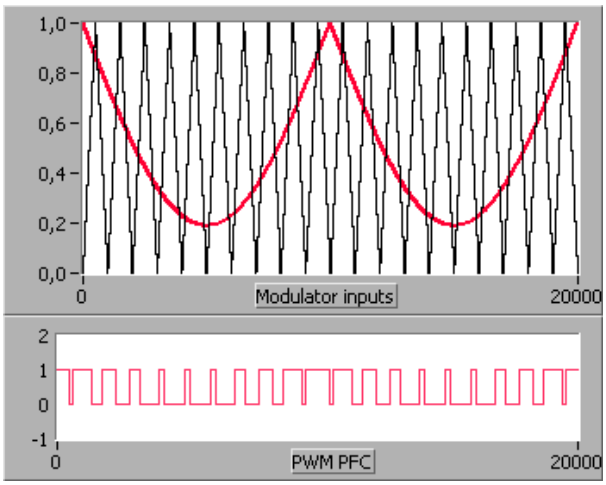
$$Iin(t) = Iin * \sqrt{2} * \sin(\omega * t)$$

$$I_{SWITCH}(t) = PWM(t) * Iin(t)$$

$$I_{FRED}(t) = (1 - PWM(t)) * Iin(t)$$

Input voltage peak to output voltage ratio is taken as variable (0<= Uinpk/Uout <=1)





The pictures are shown at 230V 50Hz AC input and 2,3kW output with 1kHz switching frequency for better visibility.

Parameter Extraction and Loss Calculation

The idea is to measure characteristic parameters of the semiconductors and use them for the calculation of the losses in the different applications.

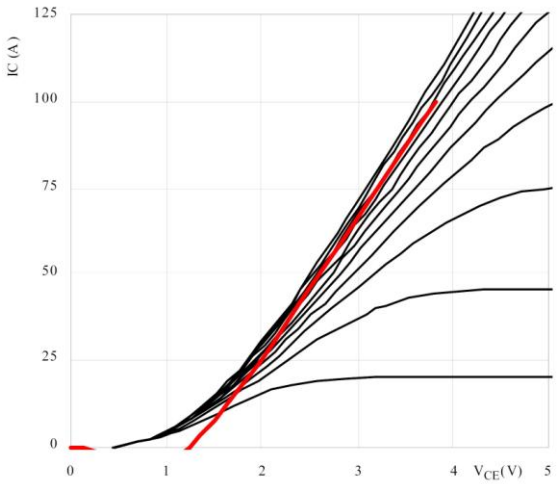
Calculation of Static Losses

The average static loss of the switch for the first half wave is:

$$Pst_{SWITCH} = 2/T * \int_0^{T/2} U_{SWITCH}(I_{SWITCH}(t)) * I_{SWITCH}(t)dt$$

Assuming linear static characteristics

$$U_{SWITCH} = Uth + rt * I_{SWITCH}$$



Therefore it is possible to describe the static characteristics with 2 parameters (Uth, rt) and use them for the calculation of static losses.

$$Pst_{SWITCH} = 2/T * \int_0^{T/2} (Uth + PWM(t) * Iin(t) * rt) * PWM(t) * Iin(t) dt$$

Using:

$$PWM^2(t) = PWM(t)$$

and using **D** as average model switch duty cycle:

$$D(t_i) = 1/T_{SW} * \int_{t_i}^{t_i+Tsw} PWM(t) dt$$

$$Pst_{SWITCH} = 2/T * (Uth * \int_0^{T/2} PWM(t) * Iin(t) dt + rt * \int_0^{T/2} PWM(t) * Iin^2(t) dt)$$

For CCM mode operation:

$$D(t) = 1 - \frac{Uinpk}{Uout} * \sin(\omega * t)$$

The Result:

$$Pst_{SWITCH} = 2/T * (Uth * Iin * \sqrt{2} * \int_0^{T/2} \sin(\omega * t) - \frac{Uinpk}{Uout} * \sin^2(\omega * t) dt + rt * Iin^2 * 2 * \int_0^{T/2} \sin^2(\omega * t) - \frac{Uinpk}{Uout} * \sin^3(\omega * t) dt)$$

$$Pst_{SWITCH} = Uth * Iin * (\frac{2 * \sqrt{2}}{\Pi} - \frac{Uinpk}{Uout} * \frac{1}{\sqrt{2}}) + rt * Iin^2 * (1 - \frac{Uinpk}{Uout} * \frac{8}{3 * \Pi})$$

The same way for the boost FRED

$$Pst_{FRED} = \frac{Uinpk}{Uout} * (Uth * Iin * \frac{1}{\sqrt{2}} + rt * Iin^2 * \frac{8}{3 * \Pi})$$

Calculation of Switching Losses

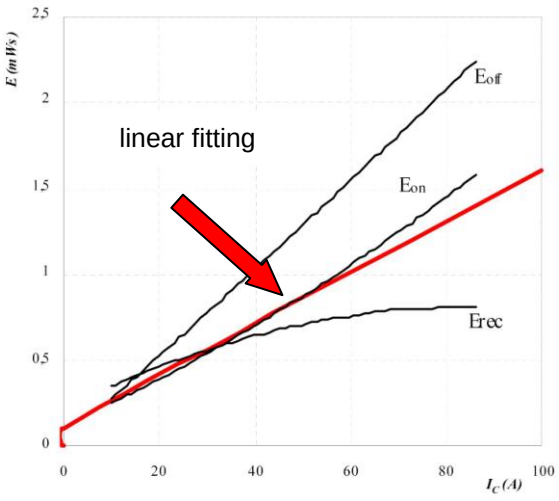
The influence of the diode for the switch on losses of the transistor makes it necessary to characterize the transistor diode pair together.

$$Psw_{SWITCH} = fsw * 2/T * \int_0^{T/2} Eoff(I_{SWITCH}(t)) + Eon(I_{SWITCH}(t)) dt$$

Assuming linear switching characteristics, it is possible to describe the switching characteristics with 4 parameters (Eoff0, Eoffn, Eon0, Eonn) and use them for calculation of the switching losses:

$$Eoff(I_{SWITCH}) = Eoff0 + (Eoffn - Eoff0)/In * I_{SWITCH}$$

$$Eon(I_{SWITCH}) = Eon0 + (Eonn - Eon0)/In * I_{SWITCH}$$



With In and Un are the nominal current and output voltage where switching losses were measured and f_{SW} is a constant switching frequency:

$$Psw_{SWITCH} = \frac{Uout}{Un} * fsw * \frac{2}{T} * \int_0^{T/2} Eoff0 + Eon0 + \frac{Eoffn - Eoff0 + Eonn - Eon0}{In} * I_{SWITCH}(t) dt$$

The switching losses are calculated to:

$$Psw_{SWITCH} = \frac{Uout}{Un} * fsw * (Eoff0 + Eon0 + \frac{Iin}{In} * \sqrt{2} * \frac{2}{\Pi} * (Eoffn - Eoff0 + Eonn - Eon0))$$

Same for the FRED:

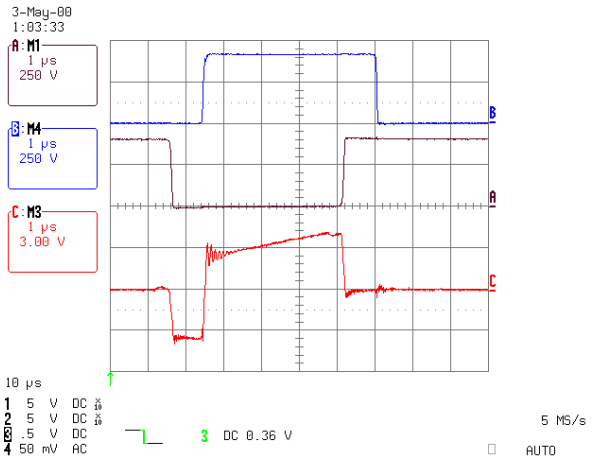
$$Psw_{FRED} = \frac{Uout}{Un} * fsw * (Erec0 + \frac{Iin}{In} * \sqrt{2} * \frac{2}{\Pi} * (Erecn - Erec0))$$

Zero-Voltage-Switching

In ZVS applications the transistor is switched on at 0V. In applications with a transformer in the output ZVS is the normal configuration. In these applications the current in the transformer will change the polarity during every switching cycle. But in that case the transistor will take over the current from the free wheeling diode at the zero crossing of the voltage. The switch on losses in this case are zero and the switching losses are only switch off losses. At switch off the situation is the same as in hard switching circuits. A low inductive DC-circuit will also here minimize the voltage overshoot and reduce the losses.

Model for calculation:

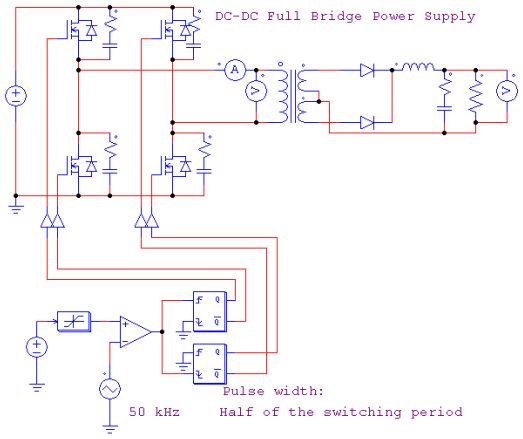
- ZVS soft switching environment
- The half bridges are not equally loaded due to asymmetry of circulating current
- Calculation like for DC applications but the variable parameter is the phase shift
- The maximum duty cycle for switch is 0,5
- Eon turn on energy is considered to be zero
- Eoff turn off energy at full load condition can be further decreased by parallel capacitors



Prediction of losses is much simpler for systems where fluctuation of variables is not present, so values averaged for a single switching cycle equal average losses. $Pst_{SWITCH} = (Uth * Iout + rt * Iout^2)/2 * \varphi$

If $0 <= \varphi <= 1$ is the phase-shift in a ZVS system

$$Psw_{SWITCH} = fsw * Eoffn * \frac{Iout}{In} * \frac{UDC}{Un}$$



Using the thermal model

This is the thermal equation describing the thermal conditions of the semiconductor.

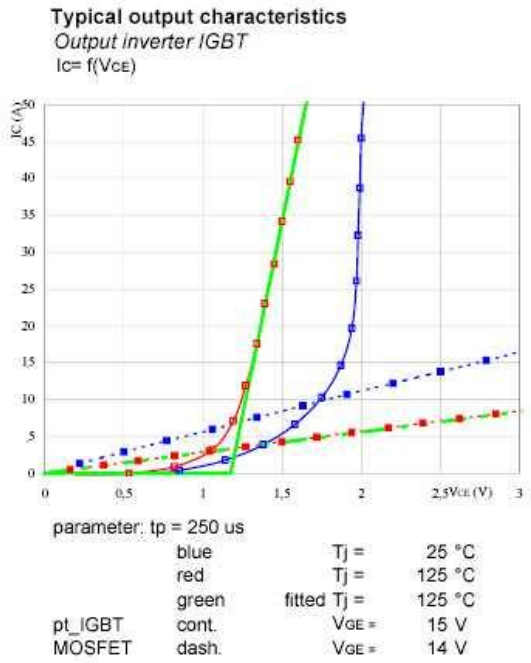
$$Ptot_{SWITCH} = Pst_{SWITCH} + Psw_{SWITCH} = \frac{Tjmax - Th}{Rthjh}$$

By fixing the T_{Jmax} temperature we can solve the equations for available current at fixed application parameters and can check the influence of semiconductor characteristic parameters for best performance.

Component Comparison

In the next section we compare the performance of components for the different applications. The 1st question is usually: "IGBT or MOS-FET?" But since different MOS-FET and IGBT technologies are available a more detailed investigation is necessary. But the principle is still valid. The IGBT has lower static losses and the MOS-FET is superior in the switching performance. Here the comparison of the static characteristics between:

- Ultrafast PT IGBT (solid line) and
- Metal Gate MOS-FET (dotted line).



Whereas the voltage drop in the MOS-FET is linear with the current is the behavior of the IGBT closer to bipolar semiconductors. At higher currents the static losses in the IGBT are only a fraction of the MOS-FET losses. The trade of is now to optimize the switching losses with the static losses. The ideal component is found when both losses are equal. It makes no sense to include standard speed IGBTs in this comparison for high frequency power applications. Only the fastest chip technologies dedicated for switching frequencies of more then 100kHz are compared:

- Metal Gate MOS-FET
- CoolMOS
- Ultrafast PT IGBT
- Metal Gate PT IGBT
- High Speed NPT IGBT

Other conditions for the comparison:

- The components for each comparison have about the same chip area.
- The max junction temperature of the chip is limited to125°C. This is important because the conditions used for the calculated are based on lifetime not the maximum values of the components. With respect to the fact that mechanics as chip solder or wire bonding are usually determine the end of life limit of the semiconductors this parameters are independent from the given chip and its manufacturer specification.
- All transistors are controlled with an additional emitter contact wire bonded directly onto the chip. This construction has the advantage that the parasitic inductance has no influence into the gate-emitter-voltage of the transistor control. If module technology is used for fast switching applications this topology provides a significant improvement with low effort.

Hard Switching in Continuous Mode PFC

Fast IGBT´s are available now and the frequency limit for the usage of IGBT´s is extended to higher frequencies. But this limit is not fixed, it differs dependent on the individual applications. The following comparison is based on a PFC-boost circuit running in continuous mode with V_{IN} / V_{OUT} = 0,8 (valid for V_{AC} = 230V and V_{OUT} = 400V:

PT Ultrafast IGBT vs. Metal Gate MOS-FET

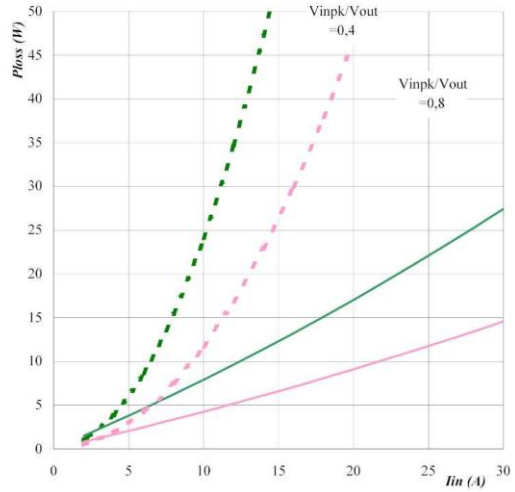
- Ultra Fast PT-IGBT (solid line) is compared with
- Metal Gate MOS-FET (dashed line):

For both transistors we use a tandem diode (2 x 300V diode in serial) as a boost diode.

Static Losses:

Typical avarage static loss as a function of input current

Switch Ploss=f(lin)

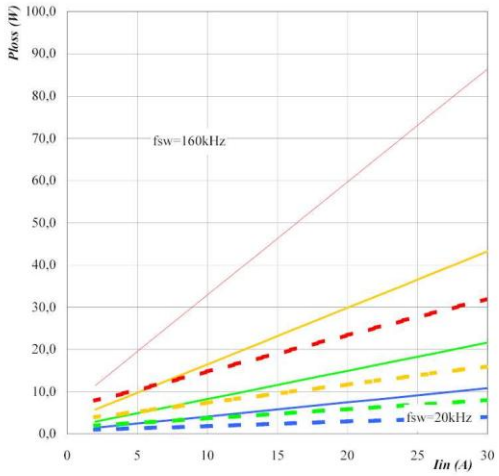


Conditions:	Tjmax=	125	°C	
Ratio of input peak to output DC voltage				
parameter	inpk/Vout from	0,4	to	0,8
	in	0,4	steps	
module 1	continuous lines			
module 2	dashed lines			

As expected the IGBT is the superior device regarding static losses. But in PFC applications often high frequencies are used so that the switching losses are the more important parameter and here the Metal Gate MOS-FET is in front:

Typical avarage switching loss as a function of input current

Switch Ploss=f(lin)

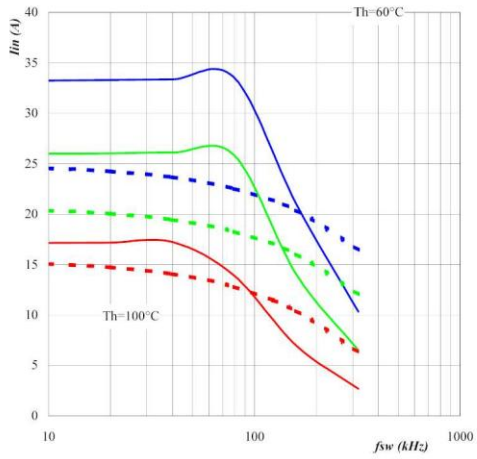


Conditions:	Tjmax=	125	°C	
Switching freq	sw from	20	kHz to	160 kHz
parameter	in	* 2	steps	
module 1	DC link=	400	V	
module 2	DC link=	400	V	

A comparison of the total available power as a function of the heat sink temperature shows what the right solution for different PWM frequencies is:

Typical available input current as a function of switching frequenc

Per boost phase Iin=f(fsw)



Conditions:	Tj=Tjmax			
Heatsink temp	Th from	60	°C to	100 °C
parameter	in	20	°C	steps
module 1 Vinpk/Vout=	0,8	DC link=	400	V
module 2 Vinpk/Vout=	0,8	DC link=	400	V

The comparison shows that the PT-Ultrafast IGBT is the better solution for up to ca. 120kHz.

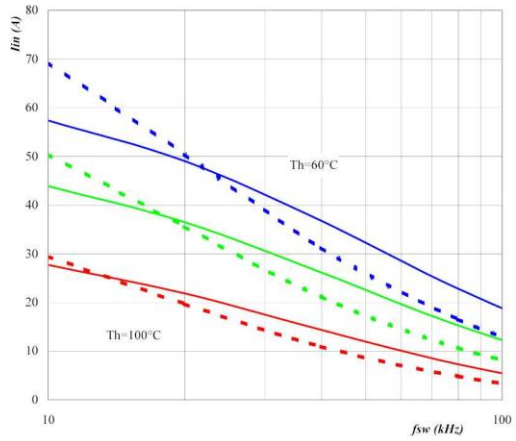
NPT High Speed IGBT vs. PT Ultrafast IGBT

The following comparison is made between:

- 2 x 30A rated paralleled High Speed NPT IGBT's (solid line) and
- single chip 60A DC rated Ultra Fast PT IGBT (dashed line).

The 2 NPT chips together have about the same chip area as the pt chip.

Typical available input current
as a function of switching frequency
Per boost phase lin=f(fsw)



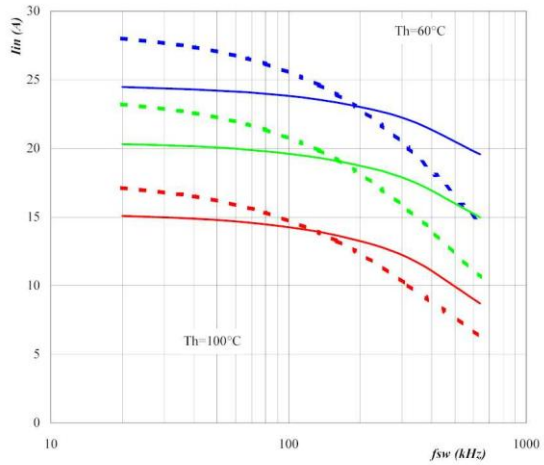
Conditions:		Tj=Tjmax			
Heatsink temp.		Th from	60 °C to	100 °C	
parameter		in	20 °C	steps	
module 1	Vinpk/Vout=	0,8	DC link=	400 V	
module 2	Vinpk/Vout=	0,8	DC link=	400 V	

Already at switching frequencies > 20kHz the NPT-High Speed is the superior device. But the overall difference is not very big.

Metal Gate MOS-FET vs. CoolMOS
The following graph compares the available output power of:

- Metal Gate MOS-FET (solid line) and
- CoolMOS (dashed line)

Typical available input current
as a function of switching frequency
Per boost phase lin=f(fsw)



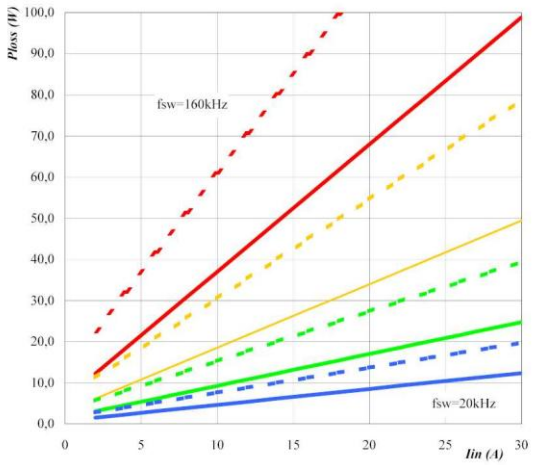
Conditions:		Tj=Tjmax			
Heatsink temp.		Th from	60 °C to	100 °C	
parameter		in	20 °C	steps	
module 1	Vinpk/Vout=	0,8	DC link=	400 V	
module 2	Vinpk/Vout=	0,8	DC link=	400 V	

Tandem FRED vs. Hyperfast FRED
Next is a comparison showing the influence of the boost diode for the system performance:
1st a comparison between:

- Tandem FRED (solid Line) and
- Hyper Fast FRED (dotted Line):

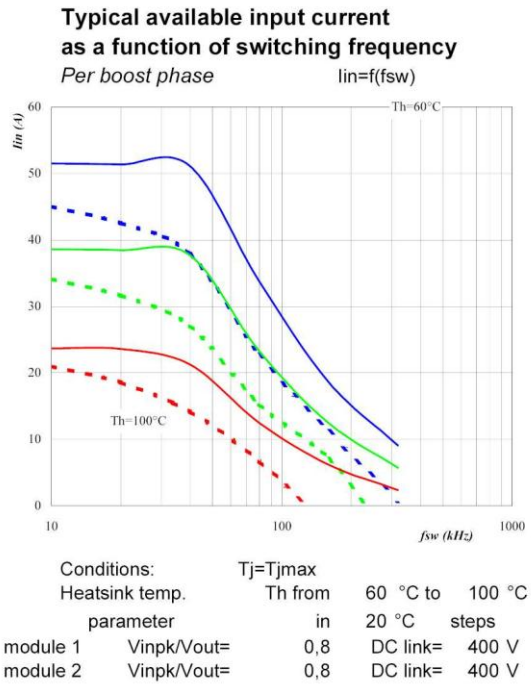
The Transistor is in both cases a Ultra fast PT IGBT.

Typical avarage switching loss
as a function of input current
Switch Ploss=f(lin)



Conditions:		Tjmax=	125 °C		
Switching freq.		fsw from	20 kHz to	160 kHz	
parameter		in	* 2 steps		
module 1		DC link=	400 V		
module 2		DC link=	400 V		

The figure shows the drastic influence of the boost diode for the switching losses of the IGBT. At f_{PWM} = 80kHz and I_{Input} = 10A the switching losses of the IGBT with the tandem FRED are 19W compared with 30W for the Hyperfast FRED.

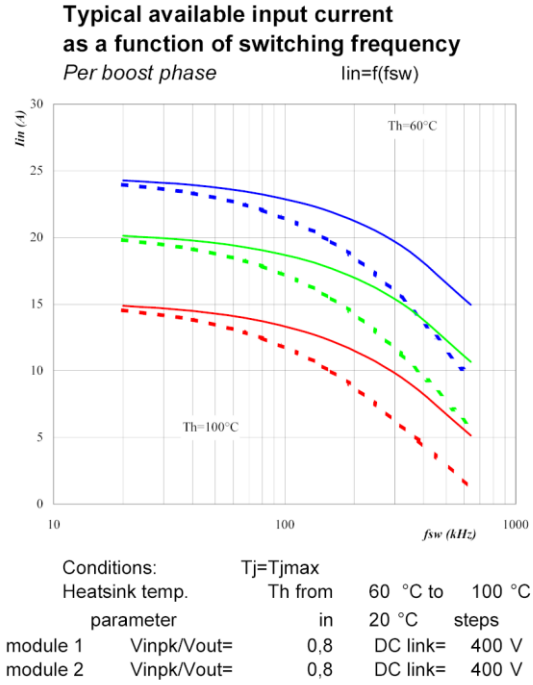


The solution with the Hyperfast FRED is able to work with an input current of ca. 20A (at 80°C heat sink and 60kHz) whereas the Tandem solution is able to accept ca. 29A at similar conditions. The transistor in both examples is the same!

SiC Rectifier vs. Tandem FRED

The next Figure shows the optimum achievable with:

- SiC-Rectifier (solid line) compared with
- Tandem FRED (dashed line):



The figure shows the available input current as function of the PWM frequency. As expected the clear advantage of the solution with the SiC-Rectifier is visible. This shows the possibility to extend the frequency range with SiC-Rectifier up to about 500kHz.

ZVS in Bridge Applications

Because of the lower importance of the freewheeling diodes at ZVS switching only the direct influence of the switching transistors are compared. In this calculation no additional snubber capacitors for loss reduction are considered.

PT Ultra Fast IGBT vs. Metal Gate MOS-FET

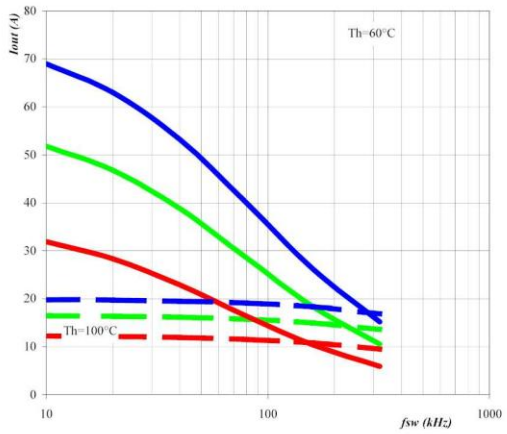
The following graph compares the available output power of:

- Ultrafast PT IGBT (solid line) compared with an
- Metal Gate MOS-FET (dashed line):

Typical available output current as a function of switching frequency

Inverter Iout=f(fsw)

Phase 1



Conditions:	Tj=125C				
Heatsink temp.	Th from	60	°C to	100	°C
parameter	in	20	°C	steps	
module 1	Ioutpk/Iout=	1,3	DC link=	400	V
module 2	Ioutpk/Iout=	1,3	DC link=	400	V
module 1	ZVS loss reduction factor			1	
module 2	ZVS loss reduction factor			1	

PT Ultra Fast IGBT vs. CoolMOS

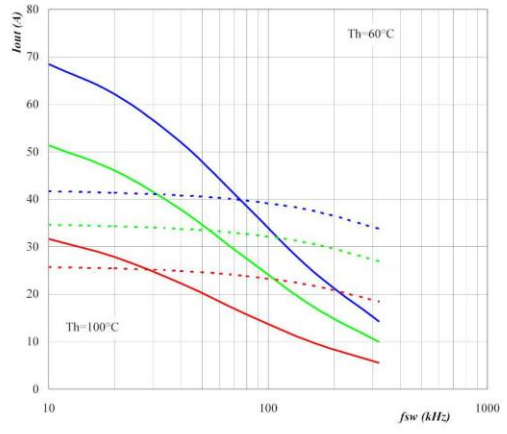
The following graph compares the available output power of:

- Ultrafast PT IGBT (solid line) compared with an
- Metal Gate MOS-FET (dashed line):

Typical available output current as a function of switching frequency

Inverter Iout=f(fsw)

Phase 1



Conditions:	Tj=125C				
Heatsink temp.	Th from	60	°C to	100	°C
parameter	in	20	°C	steps	
module 1	Ioutpk/Iout=	1,3	DC link=	400	V
module 2	Ioutpk/Iout=	1,3	DC link=	400	V
module 1	ZVS loss reduction factor			1	
module 2	ZVS loss reduction factor			1	

Metal Gate IGBT vs. PT Ultra Fast IGBT

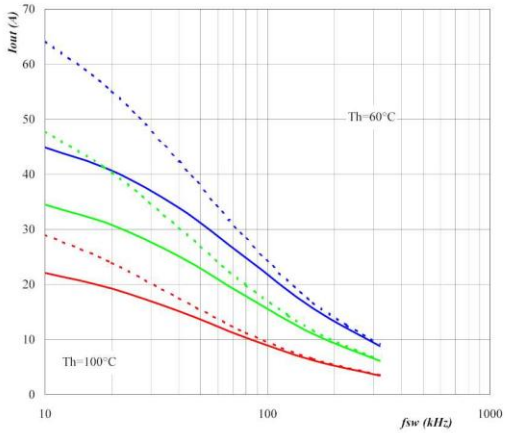
The next figure compares the available output power of :

- Metal Gate PT IGBT (solid line) compared with
- Ultrafast PT IGBT (dashed line):

Typical available output current as a function of switching frequency

Inverter Iout=f(fsw)

Phase 1

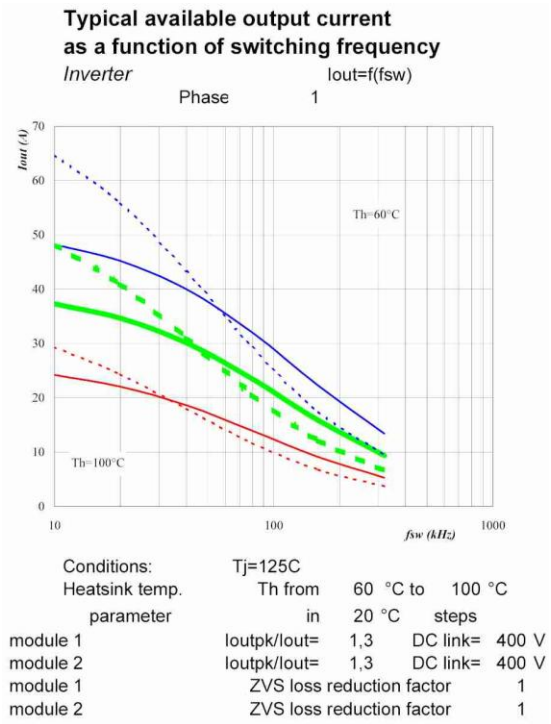


Conditions:	Tj=125C				
Heatsink temp.	Th from	60	°C to	100	°C
parameter	in	20	°C	steps	
module 1	Ioutpk/Iout=	1,3	DC link=	400	V
module 2	Ioutpk/Iout=	1,3	DC link=	400	V
module 1	ZVS loss reduction factor			1	
module 2	ZVS loss reduction factor			1	

PT Ultra Fast vs. High Speed NPT IGBT

The following comparison is made between:

- High Speed 2*30A rated parallel NPT IGBTs (solid line) and
- single chip 60A DC rated PT IGBT (dashed line):



The 2 NPT chips together have about the same chip area as the PT chip.
The continuous line shows the dual NPT and the dashed line the PT IGBT.
The green lines represent the linear approximations used for the description of characteristics.

By fixing some application parameters we can calculate the available current as a function of frequency at fixed input to output ratio or as a function of input to output voltage at fixed frequency.

Component Ranking

The components investigated have different recommended usage windows in PFC and ZVS applications.

Transistor comparison:

Component:	ZVS	PFC
Metal Gate MOS FET	> 220kHz	> 150kHz
CoolMOS	> 80kHz	> 120kHz
UltraFast PT IGBT	> 30kHz < 220kHz	> 20kHz < 150kHz
Metal Gate IGBT	> 30kHz < 220kHz	> 20kHz < 150kHz
High Speed NPT IGBT	> 30kHz < 220kHz	> 20kHz < 150kHz

PFC Boost-Diode comparison

Component:	PFC
Hyper Fast FRED	< 50kHz
Tandem FRED (2 x 300V)	> 20kHz < 200kHz
SIC – Rectifier	> 200kHz

Performance Matrix

In the following matrix the investigated components are ranked for the different switching modes and selected switching frequencies:

Hard Switched PFC - Transistor:

Switching Frequency in kHz	20 – 80	80 – 200	200 – 500
MG MOS-FET	0	++	++
Cool-MOS	+	++	+
PT – Ultrafast IGBT	++	+	-
NPT – HS IGBT	++	+	-
Metal Gate IGBT	++	+	-

Hard Switched PFC – Boost Diode:

Switching Frequency in kHz	20 – 80	80 – 200	200 – 500
SiC – Rectifier	++	++	++
Tandem FRED	++	+	0
Hyperfast FRED	+	0	-

The Performance Ranking shows that the IGBT's dominates the area below 80kHz and there is no significant advantage for a dedicated technology. At higher frequency the MOS-FET is in front. The comparison of the boost diode shows the superiority of the SiC technology. But the

high cost will reduce the today economical window for these rectifiers to frequencies > 200kHz. The tandem FRED solution offers very good performance compared with single chip hyperfast technology and the loss reduction in the transistor is already significant at 20kHz.

Bridge Configuration with ZVS:

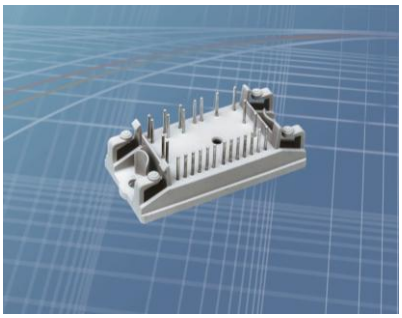
Switching Frequency in kHz	20 – 80	80 – 200	200 – 500
MG MOS-FET	-	0	++
Cool-MOS	+	++	++
PT – Ultrafast IGBT	++	++	-
NPT – HS IGBT	+	++	-
Metal Gate IGBT	+	++	-

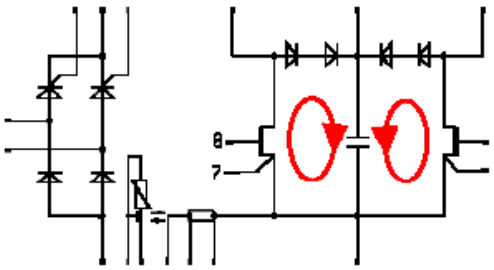
For ZVS applications also the IGBT solutions are close together. The PT ultrafast IGBT has some advantage at frequencies below 80kHz. But between 80kHz and 200kHz is no significant difference between them. The MOS-FET has an advantage at higher frequencies. The Cool-MOS is superior in ZVS applications between 220kHz and 400kHz.

Examples for the Influence of the Layout and its Parasitic Inductance for the Switching Losses

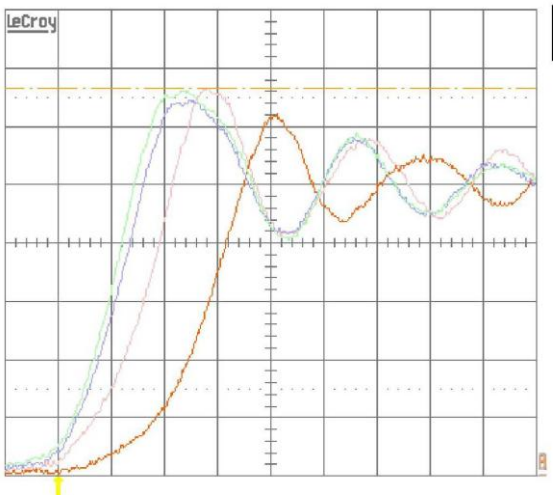
The right component selection is a must in fast switching power applications. But an optimized layout and the compensation of parasitic inductances improves the solution without extra costs. Here is an example how the short cut of parasitic inductance inside the module influences the voltage overshoot at switch off:

The module is a Tyco flowPFC 0 (P401):

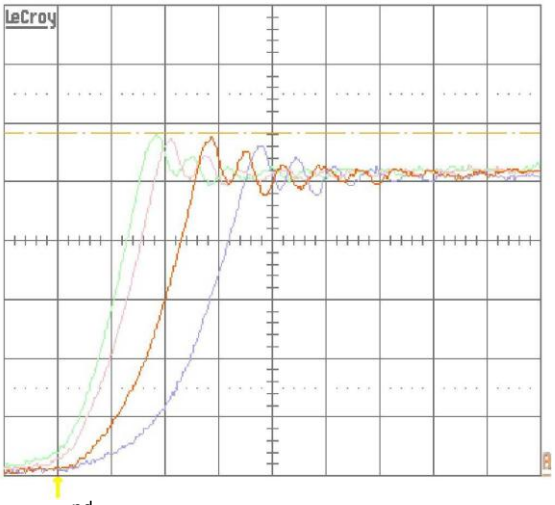




For testing the influence of the internal capacitor a measurement without and with the internal capacitor are performed.



The figure shows a PFC Module without internal capacitor. The voltage overshot reach 536V (V_{DC} =400V)



The 2nd figure shows the PFC Module with internal capacitor. The voltage overshot is now limited to 464V (V_{DC} =400V). Unfortunately it is not easy possible to measure the transistor current, when a fast capacitor is integrated next to the capacitor. But the resonance frequency is higher which indicates that the switch off slew rate is higher. This is also expected during the overshoot when the energy stored in parasitic inductance is active. The current will ramp down only after that. The switch off losses might experience an additional reduction.

Conclusion

In most cases not only one fast switching transistor is available for reaching the required performance. In hard switching applications the selection of the optimum corresponding diode is the most important factor. For hard switching and ZVS an optimized design of the power circuit is the key for performance increase without additional cost.
An intelligent module design is the best platform to implement an optimum layout and improve the efficiency to get the most out of the used components without exceeding the cost target, as:

- Selection of the right semiconductor combination dependent on the application and switching frequency. But independent of the supplier.
- Additional wire bonded control emitters for the switching transistor
- Low parasitic inductance by layout and integration of fast capacitors to short circuit the inductive loop with the lowest area.

References

- IGBT Fundamentals Siemens, May 1997