Vincotech

Flying Capacitor Inverter

Reference Design for flowFC S3 split modules

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Safety Information

This board classified as an evaluation board (EVA board) dedicated for laboratory environment only. The board should not be used for reliability testing and may not fulfill all relevant standards and requirements by the customer's country. This should be ensured by the customer.

It operates at high voltages. This board must be operated by qualified and skilled personnel familiar with all applicable safety standards.

This EVA board can endanger life by exposure to high voltages.

The device may reach high temperatures that might lead to injury.

Allow at least 4 minutes for the DC-Link capacitor to discharge to safe voltage levels (< 50 V). The voltage of the DC-link and flying capacitor always should be checked before touching the evaluation board.

This evaluation board contain ESD sensitive parts.

Failure to follow these guidelines may result personal injury or death and/or equipment damage.

Vincotech GmbH is not responsible for any damage caused by use of this evaluation board.

1 Abstract

This application note is intended to describe the EVA-LM6x/7x-FC-INV evaluation board as a simplified one phase application example for three phase flying capacitor inverter for solar market. To learn more about flying capacitor topology please, visit Vincotech's webpage. https://www.vincotech.com/support-and-documents/technical-library.

2 The power modules

To reach higher power ratings baseplate less power module with split flying capacitor topology has to be used. As a single power module can't handle the losses of this power level and hasn't got enough area for the semiconductors. The evaluation board has been designed to showcase its features. In case of split topology keeping the commutation loop in one power module has an important purpose. Otherwise the overshoots and losses would be extremely high. The power rating and the switching speed should be decreased. The commutation loops can be seen in Figure 1. The LM6x and LM7x family, which is used in this evaluation board, is designed in a way to keep the commutation loops inside one power module. While the trapezoidal pin arrangement, where all commutating pins (DC+, DC-, FC+, FC-) are at the optimal distance and the integrated capacitors results extremely low module inductance and shorter commutation loops.

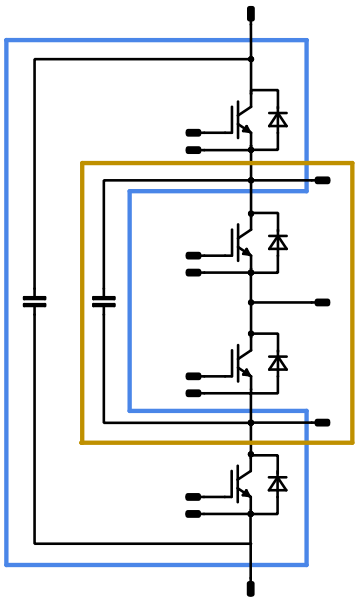


Figure 1 Commutation loops of 3-level FC inverter

The LM6x family contains the outer commutation loop (blue) with integrated flying and DC-link capacitors. The LM7x family contains the inner commutation loop (yellow) with an integrated flying capacitor. The integrated capacitors are also able to improve the switching behavior but external capacitors need to be added on the PCB for the proper operation in both position.

The modules are using Vincotech's new *flow* S3 low inductive mid-power package with enhanced thermal performance. For more information about *flow* S3 package please visit Vincotech's website.
https://www.vincotech.com/fileadmin/user_upload/content_media/documents/pdf/support-documents/technical-papers/Vincotech_TP_2020-05_Flow_S3.pdf.

The schematics of the modules can be seen in Figure 2.

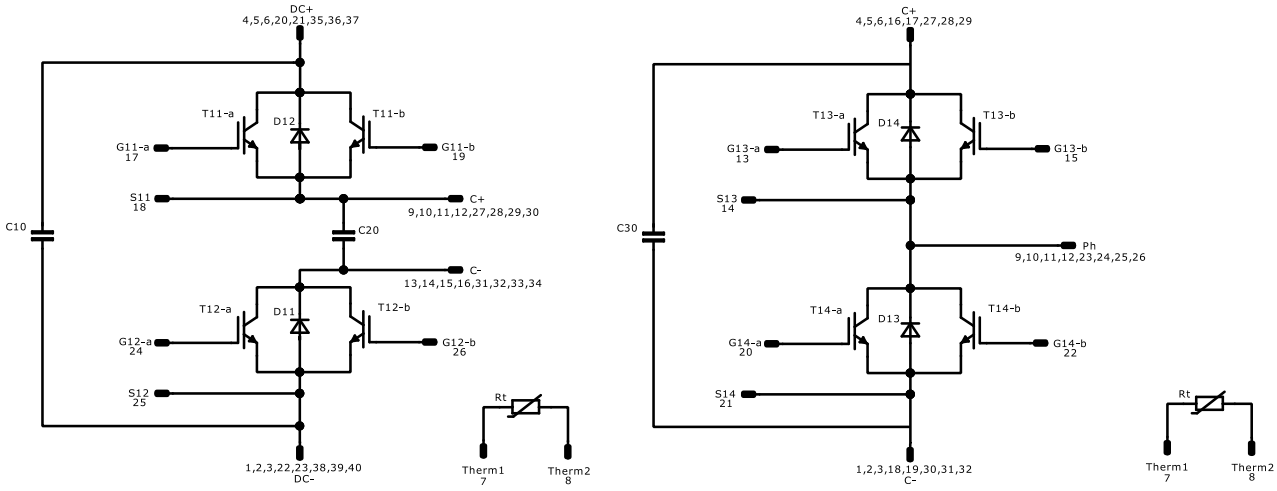


Figure 2 The LM6x and LM7x schematic

The modules can be chosen with different chip sets with different current ratings. For more detailed information please visit: https://www.vincotech.com/products.html.

3 Absolute maximum ratings

Symbol	Parameter	Conditions	Value	Unit
V_{DC}	Maximum DC input voltage		1500	V
I_{outRMS}	Maximum RMS output current	T_s = 80 °C, sinusoidal current waveform	130	A
$I_{outPeak}$	Maximum Peak output current	T_s = 80 °C	200	A
$+15\ V$	15 V supply voltage		16.5	V
T_{PCBmax}	Maximum PCB temperature		115	°C

4 The evaluation board

The evaluation board contains three different PCB cards. The drive (DRV) cards are responsible for driving the related IGBTs. As one card is able to drive one IGBT position four DRV card is needed for one phase. The control (CTR) card is responsible for the measurements, A/D conversion and contains the protection circuit. The INV card is the motherboard. It connects the flying capacitor, the DC-link capacitor, the power modules and the above mentioned PCBs. Furthermore the current sensor, the DC/DC converters and the voltage dividers can be also found on it. In this paragraph all sub-circuits will be explained in details. For more information on the used parts please visit the manufacturer's website and check the manufacturer's datasheets.

4.1 The drive (DRV) card

The DRV cards purpose is to drive the switches. The PWM signal is provided on fiber optics. On the input +15 V should be applied. The output drive signal could be either +15/-15 V or +15/0 V. As the DRV card has one channel output four cards are needed for one phase.

The input voltage is insulated by MGJ2D151505SC DC/DC converter. LED D1 indicates the presence of the +15 V_{sec}. For the insulated drive signal AFBR-2624Z fiber optic receiver is responsible. AFBR-2624Z is working with +5 V DC. Therefore an LDO (NCP718BSN500T1G) is used.

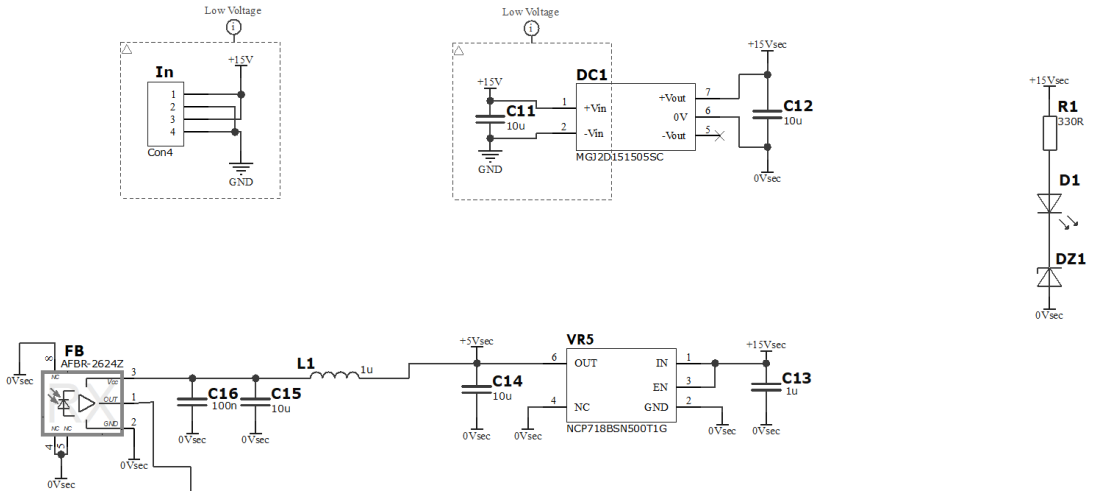


Figure 3 The input part of the DRV card

The output stage is driven by UCC27537 gate driver. The input of the gate drive is filtered by an RC filter to eliminate the noise. Another RC timer is used to provide a delay timing for the EN pin. This RC delay and the integrated UVLO protection prevent the unwanted switch ON during starting time.

The output stage of the gate driver is a MOSFET H-bridge working with +15 V DC. The gate output is connected to the second half bridge (HB2), while the emitter (source) can be connected by J1 solder jumper either to zero volt or to the first half bridge (HB1). In the first case the output will be +15/0 V, while in the second case +15/-15 V. The default setting for the jumper is the +15/-15 V configuration. The gate output of the DRV card is separated allowing flexible on and off gate resistor usage. Beside the gate resistor two additional resistors (R13, R15) are applied in the gate circuit to reduce the cross conduction current in the first half-bridge (HB1). The resistance of these two resistors (2 x 100 mΩ) are in series with the gate in case of +15/-15 V configuration and should be taken into consideration during the design. During turn ON R13 increase R_{gon}, while in case of switch OFF R15 increase R_{goff}. The gate protection elements are located on the INV card as close as possible to the gate. There can be found a TVS diode, a pull-down resistor and a gate-emitter capacitor. The gate-emitter capacitance is normally not assembled. This capacitor can clamp the voltage spike on the gate and also increases the gate-emitter capacitance to slow down the di/dt of the semiconductor.

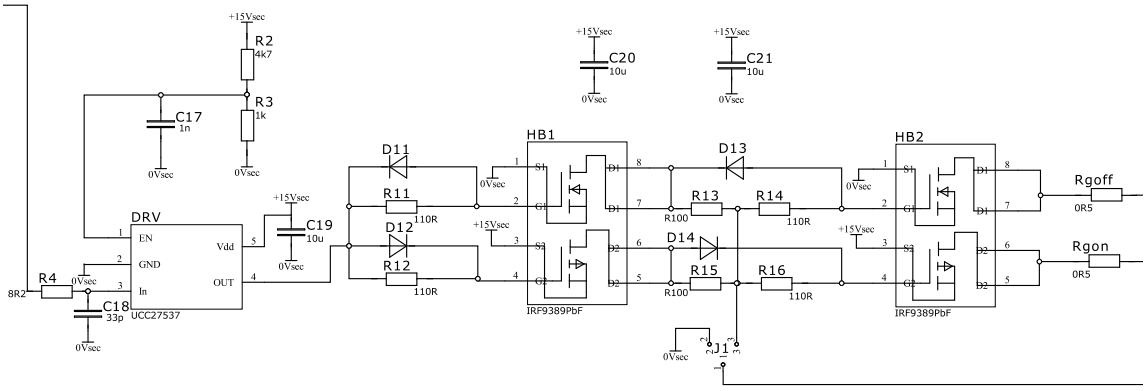


Figure 4 The output stage of DRV card

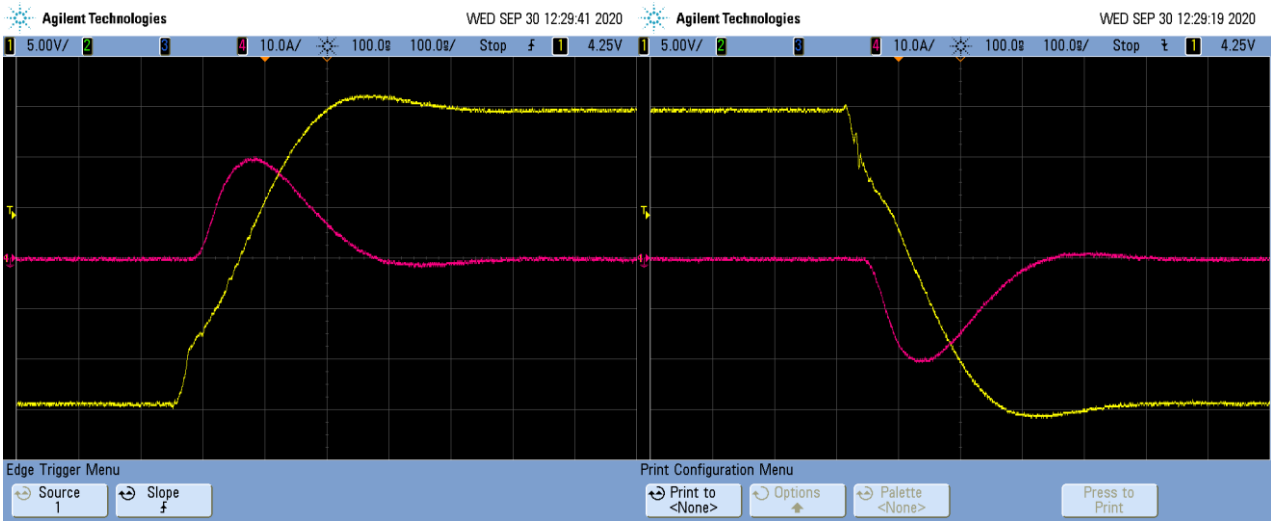


Figure 5 The output of the DRV card (CH1: gate, CH4: output current, J1 is connected to the bridge)

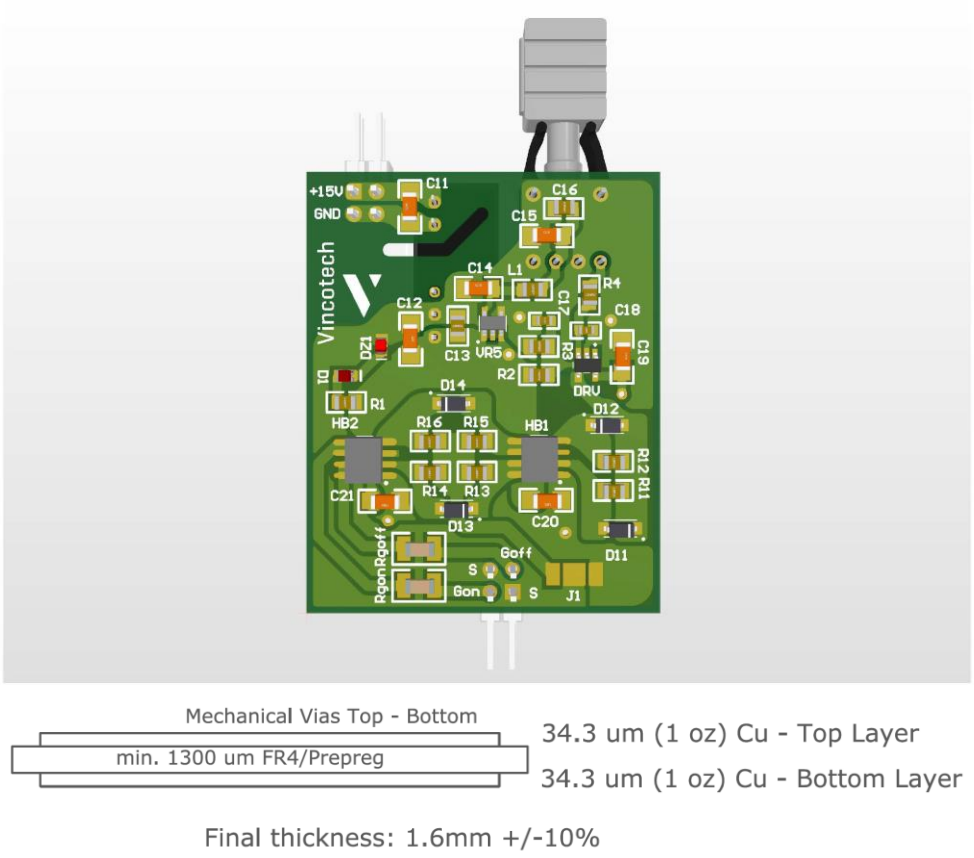


Figure 6 The DRV card

4.1.1 Characteristic Values

T_j = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$+15\,V$	15 V supply voltage		13.5	15	16.5	V
	Symbol rate of the fiber				50	MBd
λ	Optical spectrum of the fiber		630		685	nm
$t_{D_{fiber}}$	Propagation delay of the fiber			30		ns
$t_{r_{fiber}}$	Rise time of the fiber			5		ns
$t_{f_{fiber}}$	Fall time of the fiber			5		ns

$t_{Don_{DRV}}$	Turn-on propagation delay of the gate drive circuit	J1 connected to $0V_{sec}$ (1-2), f = 16 kHz, d=0.5		38,4		ns
$t_{Doff_{DRV}}$	Turn-off propagation delay of the gate drive circuit	J1 connected to $0V_{sec}$ (1-2), f = 16 kHz, d=0.5		38,2		ns
$t_{r_{DRV}}$	Rise time of the gate drive circuit	J1 connected to $0V_{sec}$ (1-2), f = 16 kHz, d=0.5		5,2		ns
$t_{f_{DRV}}$	Fall time of the gate drive circuit	J1 connected to $0V_{sec}$ (1-2), f = 16 kHz, d=0.5		12,4		ns
V_{OH}	High Output voltage of the DRV card			15		V
V_{OL}	Low output voltage of the DRV card	J1 connected to the bridge (1-3)		-15		V
V_{OL}	Low output voltage of the DRV card	J1 connected to $0V_{sec}$ (1-2)		0		V
f_{in}	Input frequency			16		kHz
I_{qu}	Quiescent current	No input is applied		48		mA

4.2 The control (CTR) card

The CTR card is responsible for the voltage, current and thermal measurements, the A/D conversion and the protection of the semiconductors.

For the stable operation an LDO (LDFM50DT-TR) is applied to stabilize the reference voltage for the A/D sigma-delta converters and for the oscillator of the thermistor. LED D1 representing the +5 V, while LED D2 the stabilized +5 V_{stab}.

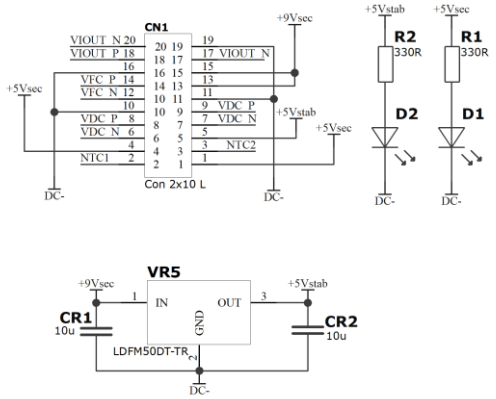


Figure 7 The input connector, the LDO and the LEDs on CTR card

For the flying capacitor and DC-link voltage measurements the voltage divider can be found on the INV card. For A/D conversions high-precision Sigma-Delta converters are used (AMC1336) in case of the flying capacitor voltage, DC-link voltage and the output current. For the reliable operation filters are applied on the input of A/D to reduce both common and differential mode noise. ClkI fiber can be used for the clock signal needed for the Sigma/Delta conversion. As this clock signal is in high frequency range the output of the A/D will be delayed compared to the input clock. Because of this delay the microcontroller could not decode the Sigma/Delta signal. This problem can be solved by ClkO fiber. ClkO transmitter sends back the clock signal to the microcontroller. As this signal will have the same delay as the output data the microcontroller will be able to decode the Sigma/Delta signal with this CLK signal. This delay can be seen on Figure 9.

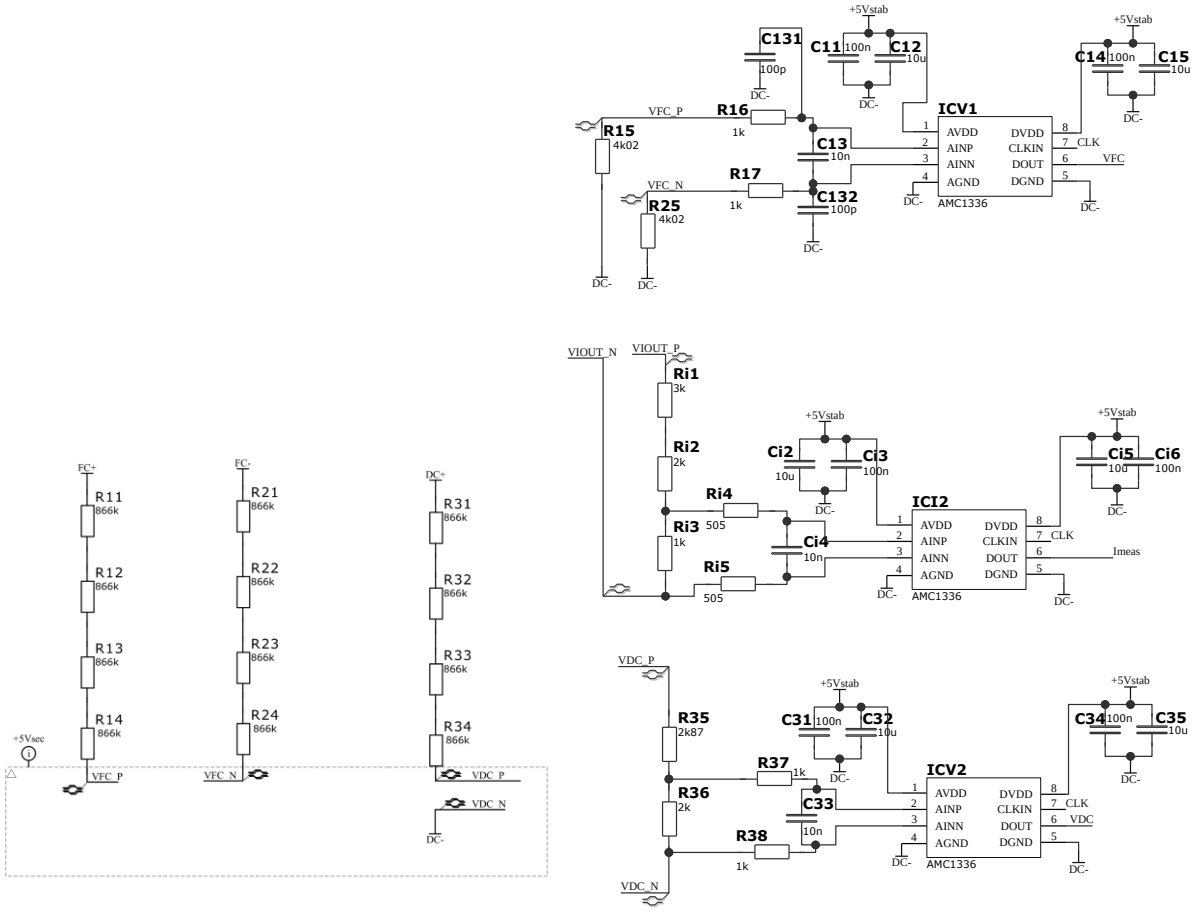
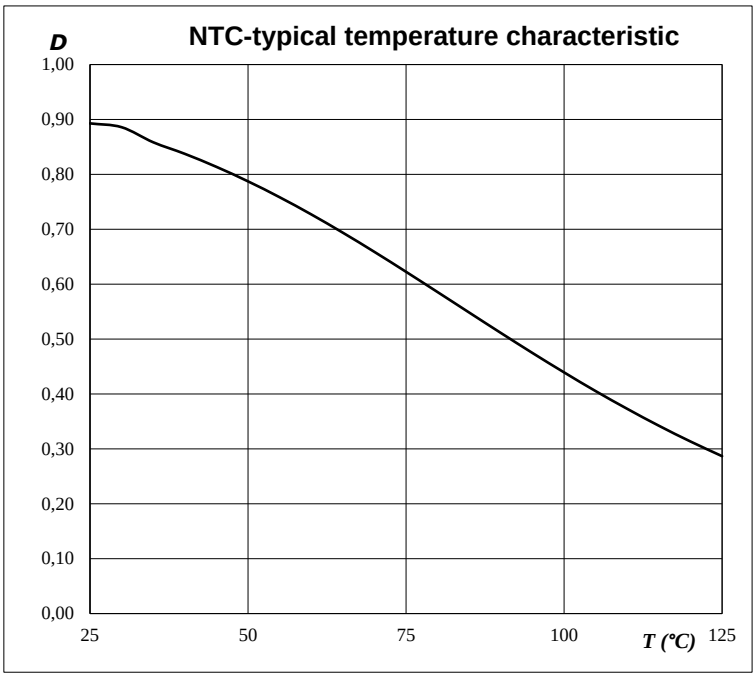


Figure 8 The A/D converters and the voltage dividers (the dividers are located on the INV card)

Figure 9 The delay between ClkI and the received ClkO on the control card on 1,6 MHz and 16 MHz

For the thermal measurement a voltage controlled pulse width modulator is used (LTC6992-1). The output frequency of the modulator is set to 100 kHz by R51 and R61. As the output duty cycle is controlled by the voltage of MOD pin, the thermistor voltage divider output is connected to that pin. As the NTC changes resistance the output duty cycle will change accordingly. The output duty cycle as function of the temperature can be seen on Figure 10. Please note that if the voltage on the MOD pin is below 5% or above 95% of the supply voltage (+5 V_{stab}), the output duty cycle will be clamped to 0% or 100%.



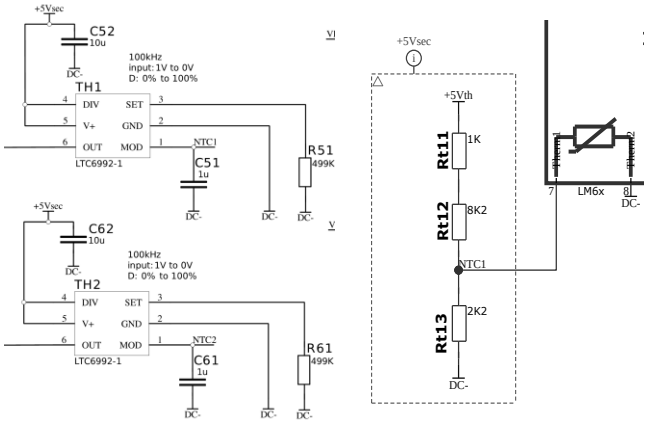


Figure 10 The thermal measurement

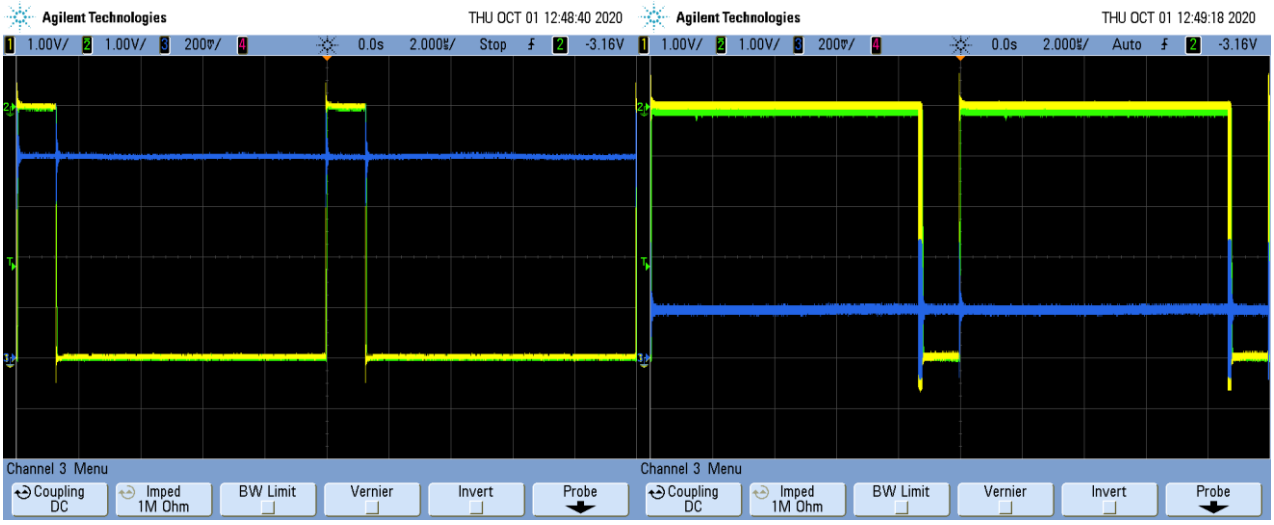


Figure 11 The thermistor output signals (CH1: TH1 output, CH2: the received signal by the microcontroller, CH3: the voltage of NTC1)

On the CTR card can be found the flying capacitor protection circuit. It consists of two negative logic fiber optics which indicates overvoltage conditions on each power module. An analog amplifier is continuously detecting the voltage of the flying capacitor. In case of too low flying capacitor voltage the voltage of the outer semiconductors getting closer to their breakdown voltage. In this case FBKL fiber will change the state to zero. If the voltage of the flying capacitor is too high an overvoltage condition will be present on the inner half-bridge. Above the upper threshold FBKH Fiber will change the state to zero. If any of this two fibers changes the state to zero the microcontroller have to stop the system as soon as possible. This protection should be included on the control side hardware or software. After the safety stop the voltage divider of the pre-charge (will be detailed later) will stabilize the voltage of the flying capacitor. As zero output indicates failure mode in case of any failure with the optic fiber the inverter will be stopped by the above mentioned protection logic.

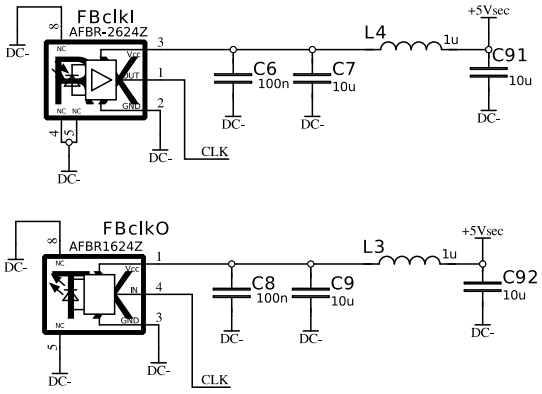


Figure 12 The fibers

The working of the safety circuit is the following. AD8237 (A1) differential instrumentation amplifier amplifies the flying capacitor voltage by the gain of three. K1 dual comparator (TLV7042) compares this signal to the voltage proportional to the DC-link voltage. If VDC is greater than three times the VFC FBKL fiber will change the state to zero. After the control card receives this failure signal the inverter must be stopped. So the flying capacitor voltage can't go below one third of the DC-link voltage. K1 also compares the flying capacitor voltage to 3 V. In this case if 3xVFC is above 3 V FBKH fiber will eject failure signal. The safety stop should be realized on the control side in the hardware or in the software. The maximum voltage can be calculated as:

$$V_{FCdiv} = 1{,}15916\ \frac{mV}{V}$$

And K1 referring 3 V to the 3xVFC.

$$V_{FCKH} = \frac{1\ V\ \cdot 1000}{1{,}15916\ \frac{mV}{V}} = 862{,}69367\ V$$

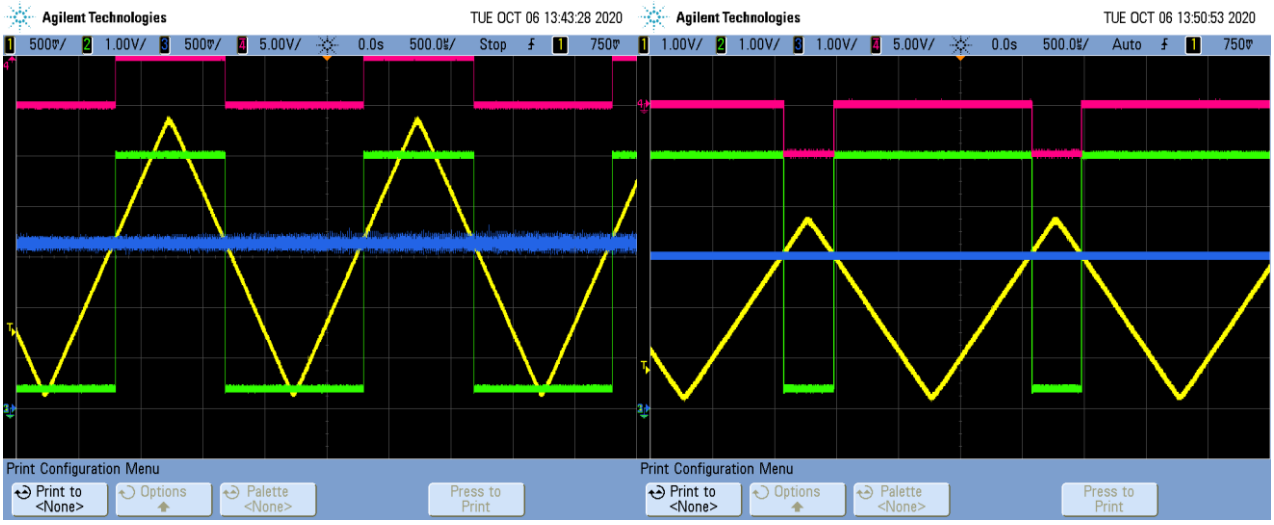


Figure 13 The output of the flying capacitor protection circuit:

- a, under voltage (CH1: 3xVFC, CH2: comparator output FCL, CH3: VDC, CH4: received signal by the microcontroller)
- b, overvoltage (CH1: 3xVFC, CH2: comparator output FCH, CH3: 3 V, CH4: received signal by the microcontroller)

Name	Function
FBclkI	the input clock signal for the sigma-delta converters
FBclkO	the recurring clock signal to eliminate the delay between the incoming and outgoing signal
FBFC	the flying capacitor voltage Σ/Δ converter output
FBDC	The DC-link voltage Σ/Δ converter output
$\overline{\text{FBKH}}$	protection, overvoltage on the flying capacitor
$\overline{\text{FBKL}}$	protection, under voltage on the flying capacitor
FBI	the output current Σ/Δ converter output

Table 1 The fibers of the CTR card

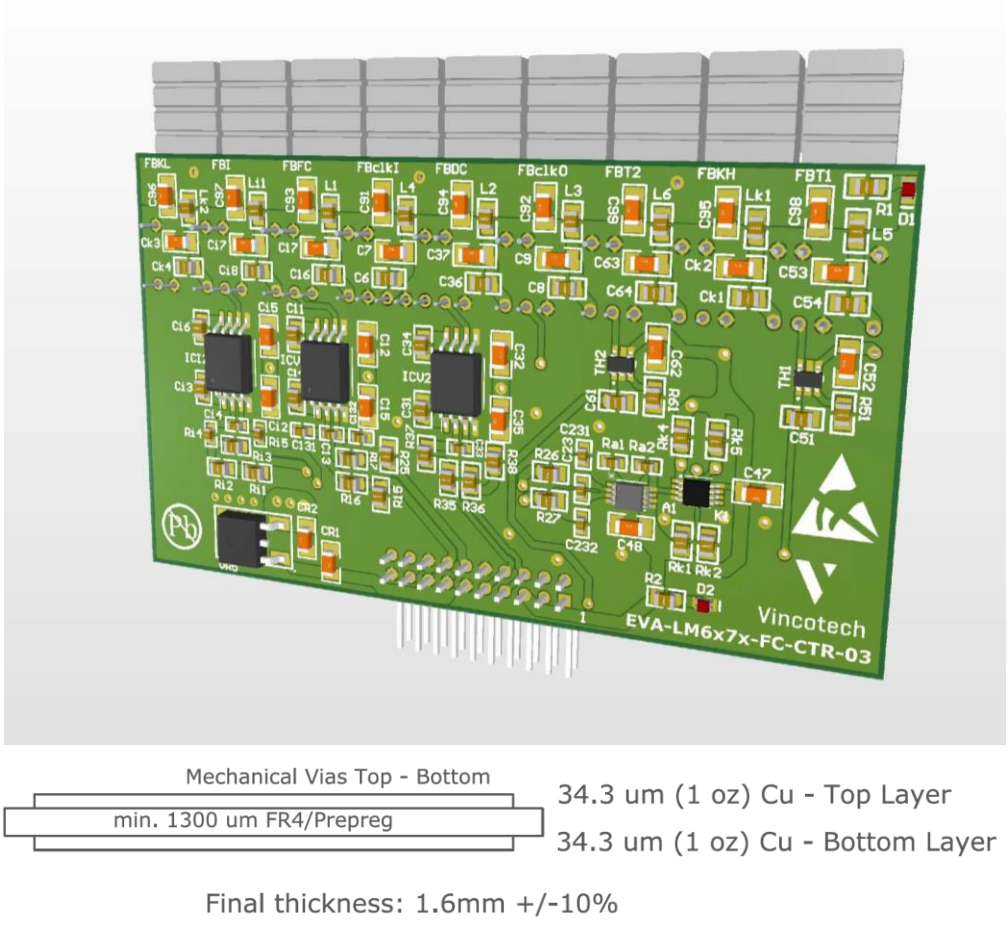


Figure 14 The CTR card

4.2.1 Characteristic Values

T_j = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{DCdiv}	Output of the flying capacitor divider			0,57656		mV/V
V_{FCdiv}	Output of the DC-link divider			1,15916		mV/V
	Resolution of the A/D		16			Bit
f_{CLK}	Clock frequency for the A/D		9	16,6	21	MHz
D_{CLK}	Duty cycle of the CLK for A/D		40%	50%	60%	
f_{FBT1}, f_{FBT2}	Output frequency of temperature reference signals			100		kHz
$t_{D_{fiber}}$	Turn-on propagation delay of the fiber			30		ns
$t_{r_{fiber}}$	Rise time of the fiber			5		ns
$t_{f_{fiber}}$	Fall time of the fiber			5		ns
$t_{r_{prot}}$	Rise time of the protection circuit output			44		ns
$t_{f_{prot}}$	Fall time of the protection circuit output			4,9		ns

4.3 The inverter (INV) card

The INV card is the mother board of the inverter. The power modules, the flying and DC-link capacitors, the DRV and CTR cards, the current sensors, the voltage dividers, the pre-charge resistors and the insulated DC/DC converters can be found on the INV card.

From the incoming +15 V two insulated DC/DC converter creates the secondary voltage levels. One is responsible for the +5 V while the other is for +9 V. The +5 V rail is used for the logical circuits, while from the +9 V rail an LDO (LDFM50DT-TR) creates stable reference for the current sensor.

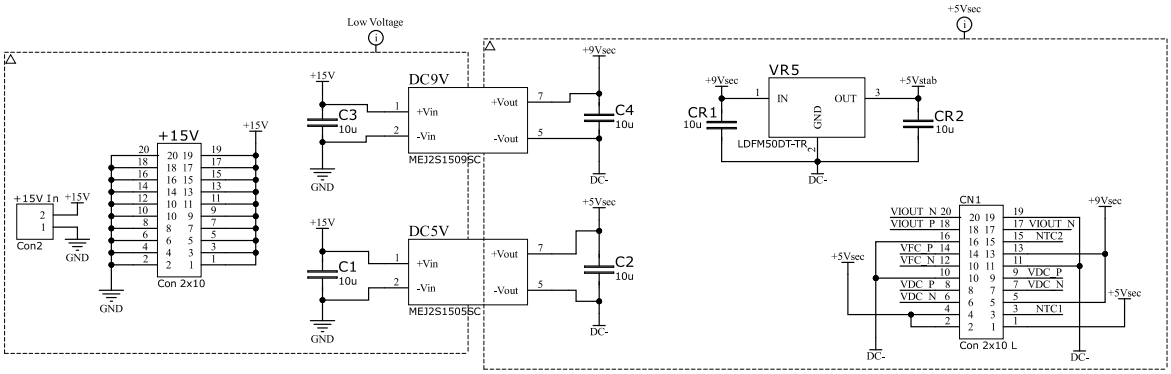


Figure 15 the input stage with the DC/DC converters, the LDO and the CTR card connector

ACS772ECB-200B is bidirectional Hall effect based insulated current sensor. The maximum peak current is +/-200 A.

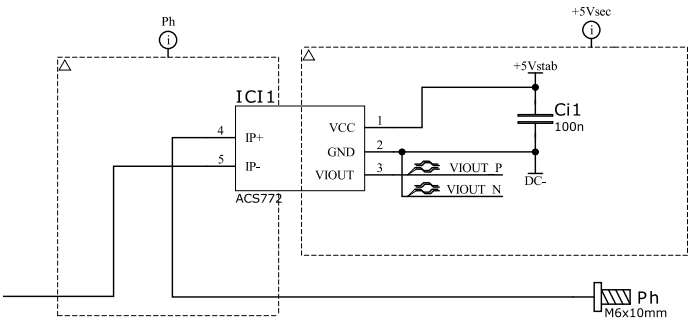


Figure 16 The current sensor

4.3.1 Startup

Before starting up the evaluation board the flying capacitor should be charged to the half of the DC-link voltage. This evaluation board uses passive pre-charge. A resistive voltage divider is used on the input to charge the flying capacitor to the correct voltage level before startup. As the voltage divider will have a power dissipation during normal operation high values should be used. However the startup time also depends on the resistance, so the higher the resistance the longer the startup. The voltage divider used for measurement have also an effect for the flying capacitor voltage. This is also balanced by the pre-charge resistors.

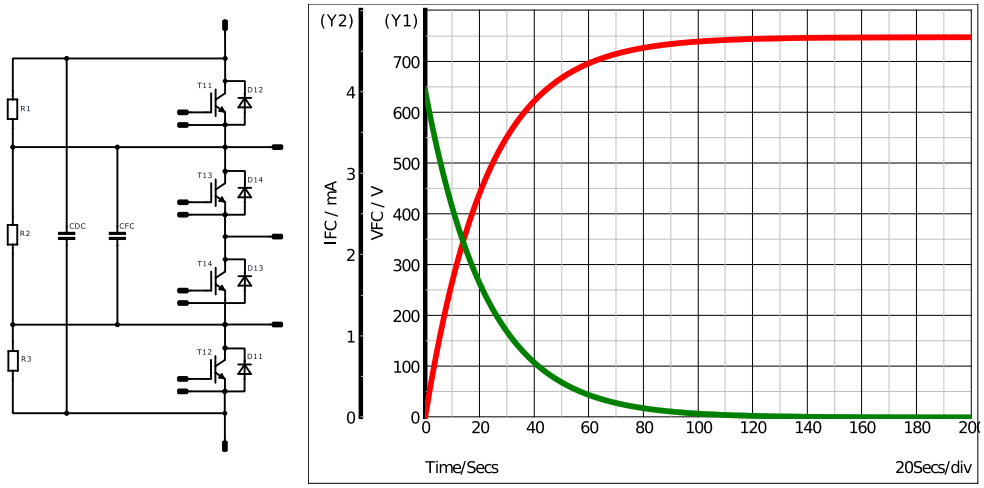


Figure 17 The pre-charge

The voltage of the flying capacitor in the function of time can be calculated with the following formula (if $R_2 = R_1 + R_3 \; and \; R_1 = R_3$, the measurement divider compensation is neglected):

$$v_{FC}(t) = \frac{V_{DC}}{2} - \frac{V_{DC}}{2} * e^{-\frac{t}{\frac{R_2}{2} * C}}$$

, where the time constant

$$\tau_1 = \frac{R_2}{2} * C_{FC}$$

4.3.2 Capacitor sizing

The voltage supplied by the flying capacitor has a key role in this topology. To keep the voltage ripple of the capacitor low suitable capacitor size is needed. To determine the minimum needed capacitance the switching frequency, the output current and the maximum allowed voltage ripple need to be considered. The size of the capacitance can be calculated as:

$$C_{FCmin} = \frac{I_{peak}}{\Delta V_{FC} \cdot 2 \cdot f_{SW}}$$

, where ΔU_{FC} is the maximum allowed voltage ripple, I_{peak} is the maximum current, f_{SW} is the switching frequency of the transistors.

For the capacitor sizing not only the needed capacitance but also the maximum allowed peak and RMS current should be considered. While the ESR and ESL values should be as low as possible.

4.3.3 Characteristic Values

T_j = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{DC}	DC input voltage			1250	1500	V
$+15\,V$	15 V supply voltage		13.5	15	16.5	V
$I_{OUTpeak}$	Peak current of the current sensor		-200		200	A
	Sensitivity of the current sensor	$I_{Opeakmin}<I_o<I_{Opeakmax}$		10		$\frac{mV}{A}$
V_{Iout0}	Zero current output voltage			2,5		V
C_{DC}	DC-link capacitor			120		µF
C_{FC}	Flying capacitor			120		µF
V_{CFC}, V_{CDC}	Maximum FC and DC capacitor voltage				1500	V
$V_{ISODC/DC}$	DC/DC isolation voltage				5,2	kV
I_{qu}	Quiescent current	No input is applied		120		mA
I_{qu}	Quiescent current	Only CLK is applied		140		mA

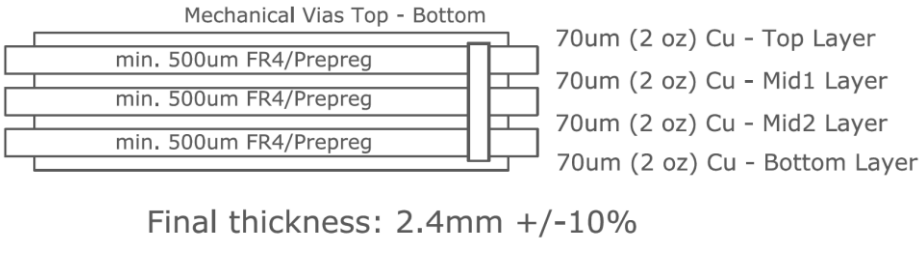


Figure 18 Layer stack of INV card

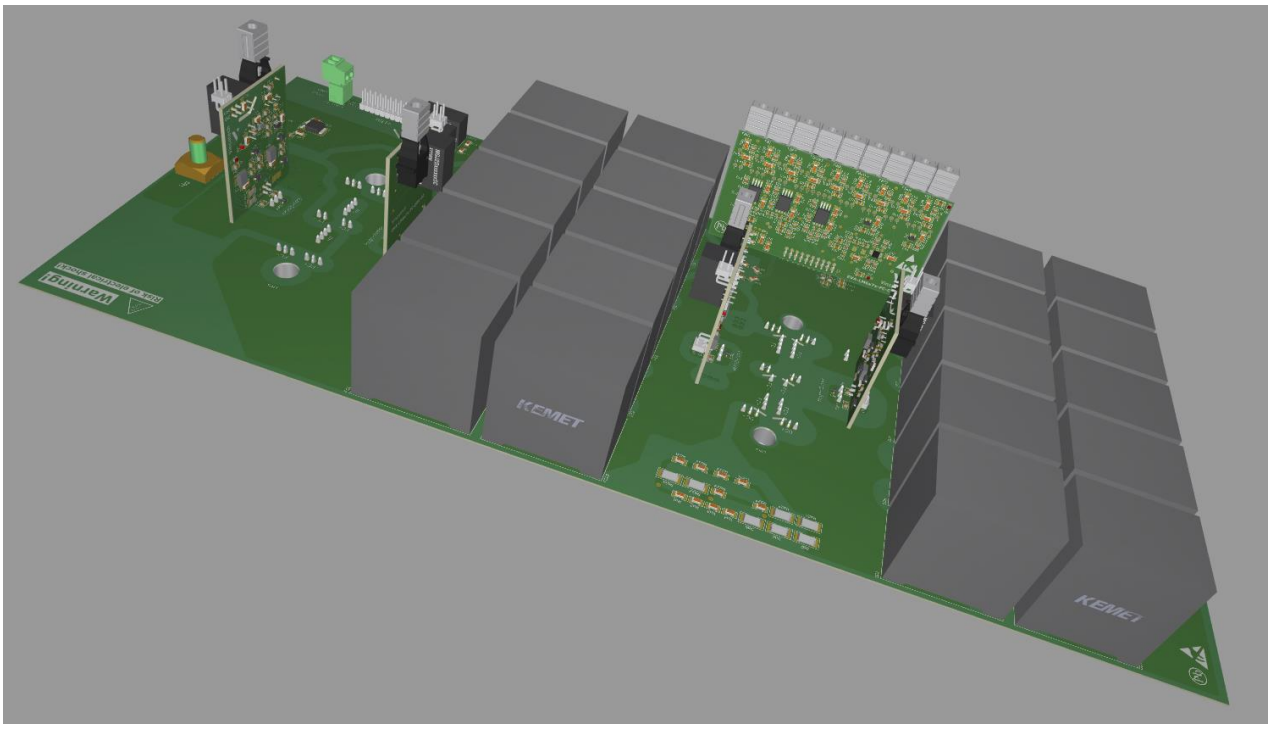


Figure 19 The Evaluation board

4.4 PCB design

To reach optimal switching behavior the PCBs has been designed with the following design criteria. The overlapping layers has been designed to maximize capacitive coupling of the power plane pairs (e.g.: DC+ to DC-, FC+ to FC- , +5 V_{sec} to 0 V_{sec}) and minimalizing the capacitive coupling to other planes.

On the INV card all high current traces are on two layers to increase the current capability. As outer layers have better thermal properties high current traces are placed both on an outer and on an inner layer to ensure symmetry in of positive and negative feed. DC- and FC- can be found on the top layer and Mid2 layer. While DC+ and FC+ can be found on the bottom layer and Mid1 layer. This alternating arrangement increase the capacitive coupling as well.

The measured signals (except the thermistor) are routed in differential mode. This can eliminate the common mode noise from the measurements. All measured signals are shielded with DC- both on own layer and on the upper and lower layer. The gate potentials are shielded with the emitter potential.

To increase the Creepage distance PCB cutouts are used.

On the inner layers smaller distance can be used. To ensure the insulation capability of the board high voltage test was applied. The minimum breakdown voltage of the INV card is 5 kV between FC+ and FC- while 8 kV between DC+ and DC-.

The copper thickness of the PCB should be chosen based on the required current capability and the usable track width. To ensure the current capability of the INV card, high current test was applied (150 A DC), where all high current trace was shorted and the temperature of the card was measured with IR camera and thermocouple.

5 Flying capacitor balancing

Balancing the flying capacitor has an important role in this topology. For the appropriate operation of the inverter the Flying Capacitor voltage has to be half of the input voltage. For the voltage regulation the input voltage, the flying capacitor voltage and the output current direction should be considered. The effect of the possible transistor states in the function of the output current direction can be seen on Table 2.

Mode	Output	Transistors				FC voltage	
		T11	T13	T14	T12	Positive output current	Negative output current
Mode 1	DC+	ON	ON	OFF	OFF	No effect	
Mode 2	Neutral	ON	OFF	ON	OFF	Increasing	Decreasing
Mode 3	Neutral	OFF	ON	OFF	ON	Decreasing	Increasing
Mode 4	DC-	OFF	OFF	ON	ON	No effect	

Table 2 Output and FC voltage states

The balancing of the flying capacitor voltage can be achieved by modifying the PWM signals. Where the duration of the neutral states have to be modified resulting the flying capacitor voltage change. To change the duration an offset have to be added to one of the modulation signals. Resulting one of the neutral state will be longer. To keep the same duty cycle on the output the inverse of the offset have to be added to the other modulation signal to shorten the other neutral state. This way the output average voltage remains the same and the flying capacitor voltage will change. This can be seen in Figure 20, which contains the original and the modified waveform with offset. The effect of the offset depends on the current direction. If the direction of the current is changing the effect of the offset will change direction accordingly.

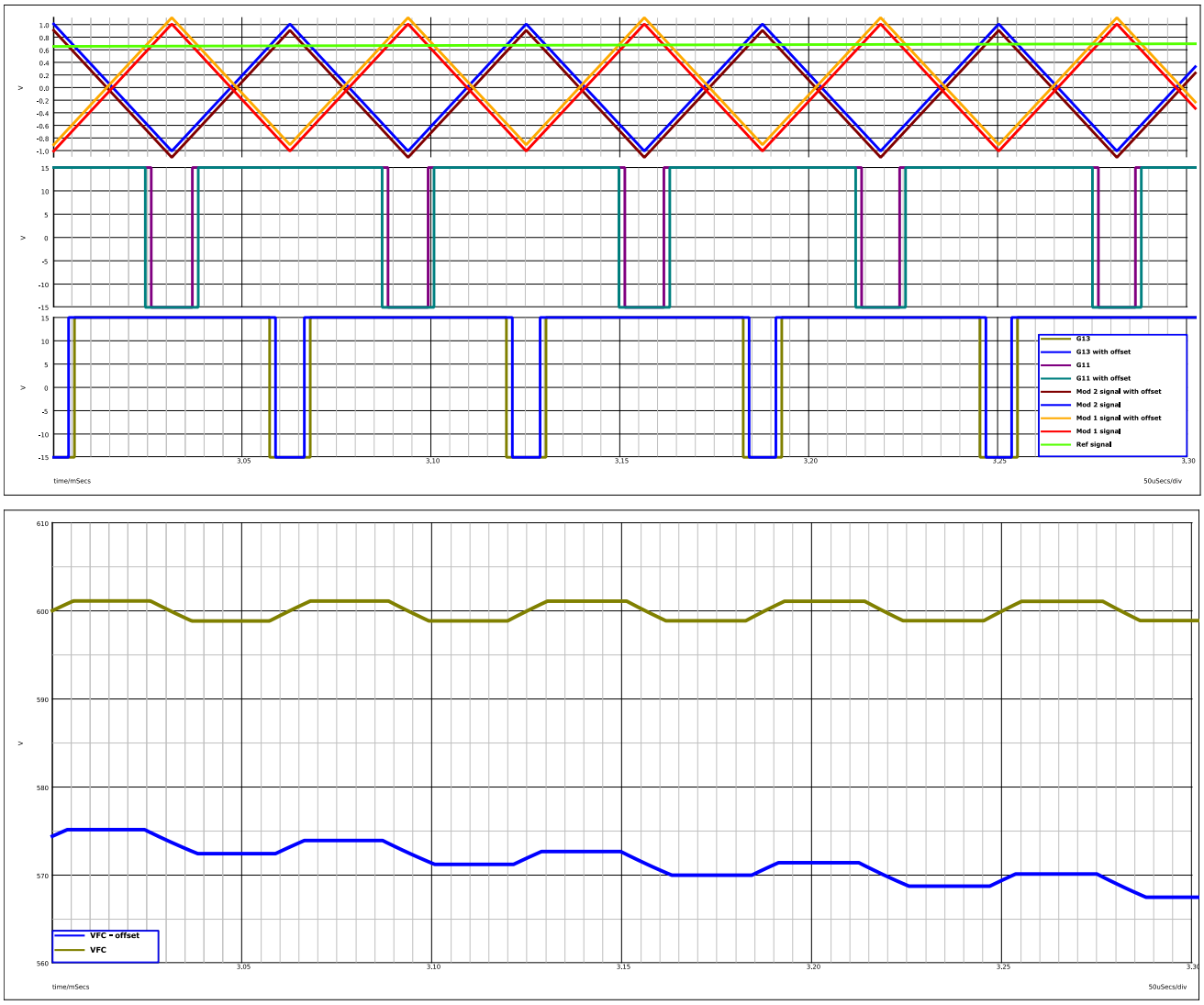


Figure 20 changing the flying capacitor voltage with offset

Based on this phenomena the regulation of the flying capacitor can be seen on Figure 21. The input reference of the regulation is $\frac{V_{DC}}{2}$. The input of the PI controller is the difference between the reference and the feedback (V_{FC}) signals. The polarity of the control output signal depends on the current direction. The duty cycle of the outer half-bridge can be calculated as the sum of the actual inverter duty cycle and the output of the regulation loop, while the inner half-bridge is the difference of those.

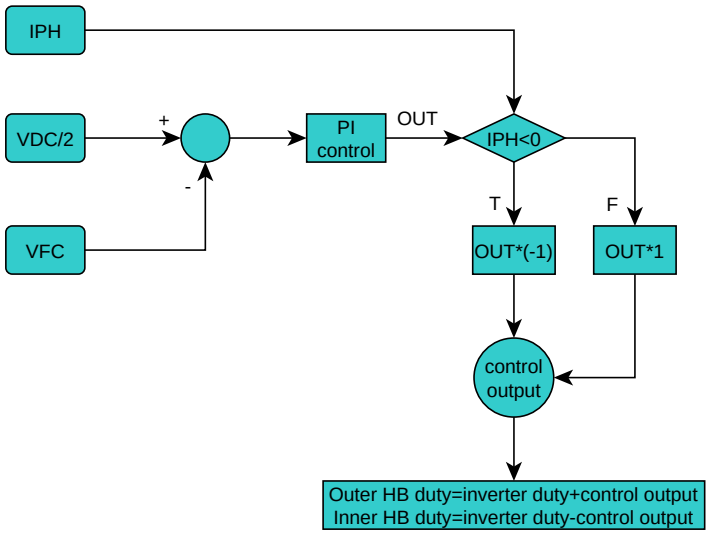
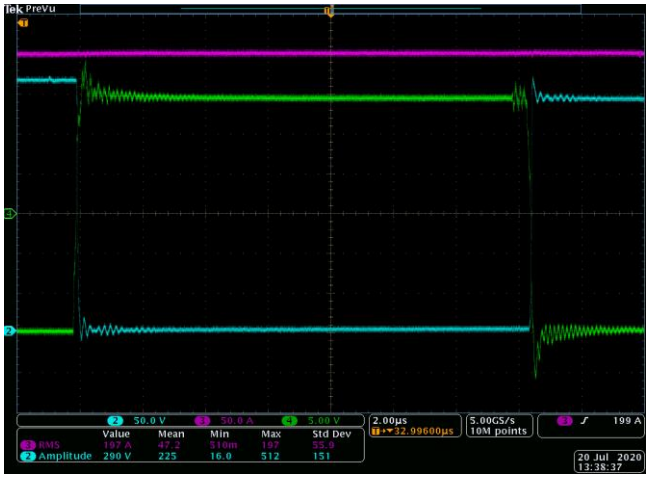


Figure 21 The flying capacitor regulation loop

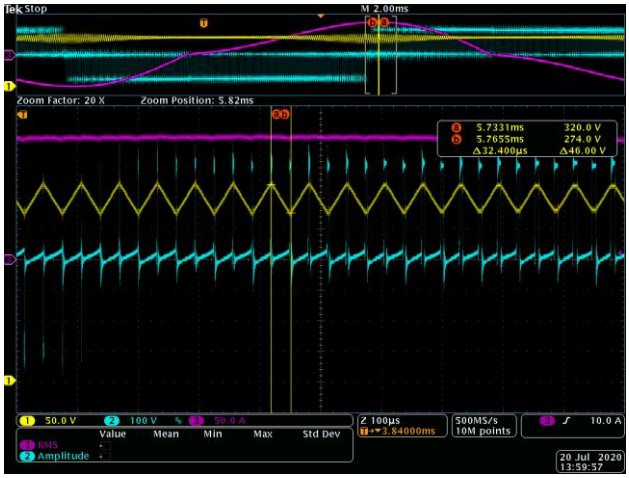
More information can be found about the balancing method of the flying capacitor on Vincotech's web site: https://www.vincotech.com/fileadmin/user_upload/content_media/documents/pdf/support-documents/technical-papers/Vincotech_TP_Solar_The_Advantages_and_Operation_of_Flying_Capacitor_Inverter_2020.pdf.

6 The measurements of the evaluation board

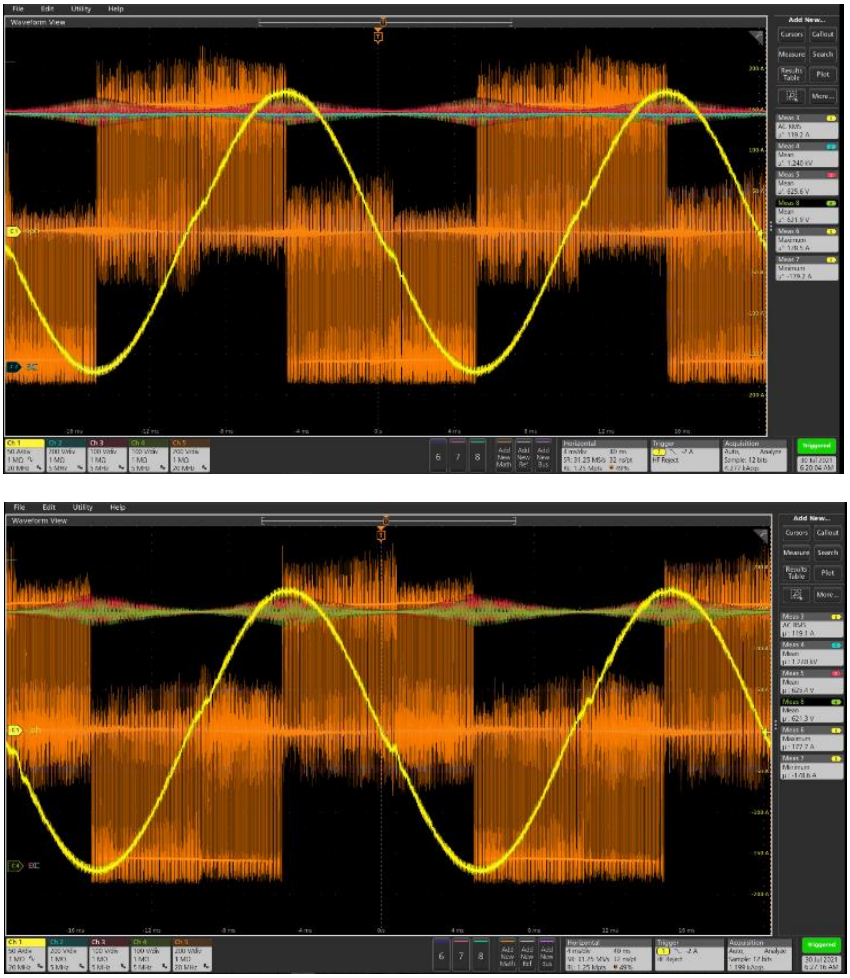
The evaluation board was measured in a one phase circulator setup. In circulator mode two inverters are connected back-to-back. One of them is the AC power source and the other is the AC power sink. This is an easy way to test more than 40 kW per phase with limited input and output capability in the laboratory. As the measurement only consists of one phase an external DC-link capacitor had to be used. This external capacitor can be eliminated in case three phase system where the input power is constant. The typical waveforms of the evaluation board can be seen on Figure 22.



T14 collector-emitter (CH2), gate-source (CH4) voltage and the output current (CH3)

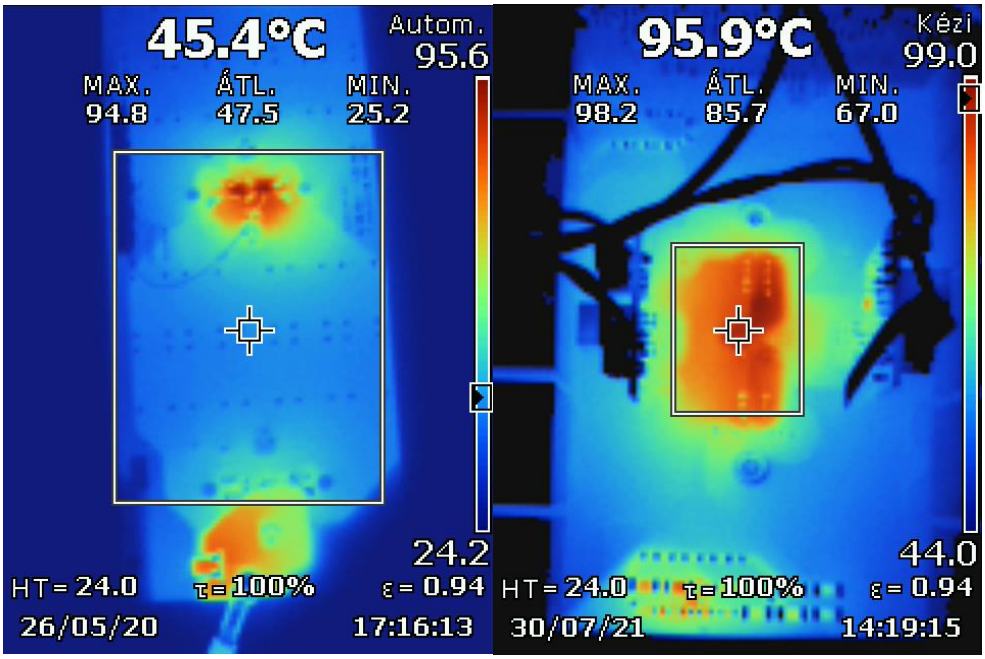


Output voltage (CH2) and current (CH3), flying capacitor voltage (CH1)



The output current (CH1), the DC-link voltage (CH2) and the flying capacitor voltage (CH3)

Figure 22 Typical waveform of the evaluation board



The temperature of the PCB with 150 A DC current (T_a= 25 °C)

The temperature of the evaluation board during normal operation (I_{outRMS}=120 A, V_{outRMS}=350 V, T_s=80 °C, T_a= 25 °C)

Figure 23 Temperature of the evaluation board

6.1 Efficiency

The following calculation was based on the circulator measurements. The result of this measurement is valid for the whole system (two inverters, inductance, DC-link capacitor bank). It is assumed that the losses of one inverter is the half of the sum losses. As in three phase application the input capacitor bank can be eliminated the evaluation board is able to reach higher efficiency in this case.

$$P_{loss_{cir}} = V_{DC} \cdot I_{DC} = 1250\,V \cdot 1{,}47\,A = 1837{,}5\,W$$

$$P_{out} = V_{outRMS} \cdot I_{outRMS} = 353{,}55\,V \cdot 119{,}2\,A = 42143{,}56\,W$$

$$P_{in_{circ}} = P_{loss_{cir}} + P_{out} = 43981{,}06\,W$$

$$\eta_{cir} = \frac{P_{out}}{P_{in_{circ}}} \cdot 100\% = \frac{42143{,}56\,W}{43981{,}06\,W} \cdot 100\% = 95{,}82\,\%$$

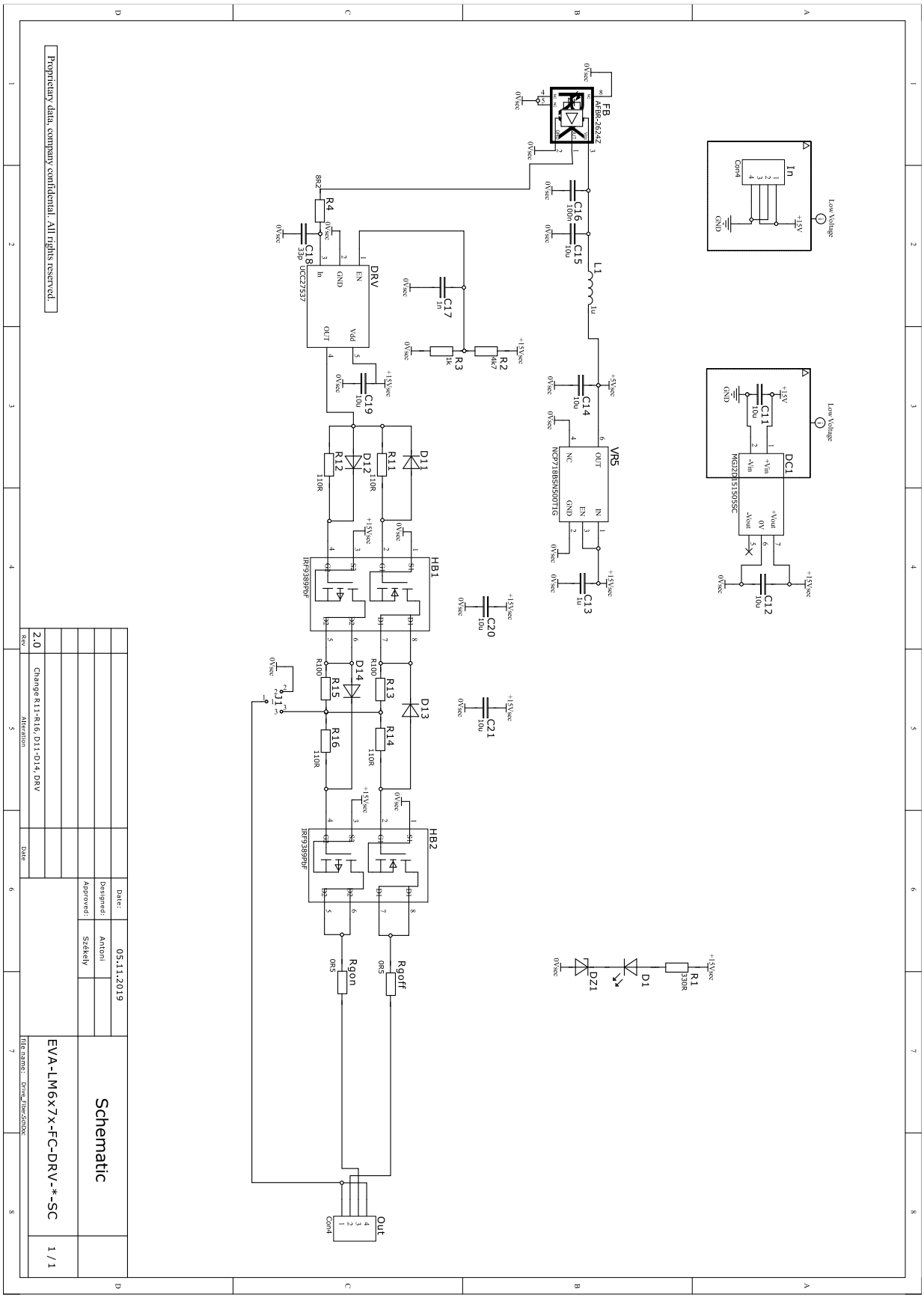
$$P_{loss_{inv}} \approx \frac{P_{loss_{cir}}}{2} = \frac{1837{,}5\,W}{2} = 918{,}75\,W$$

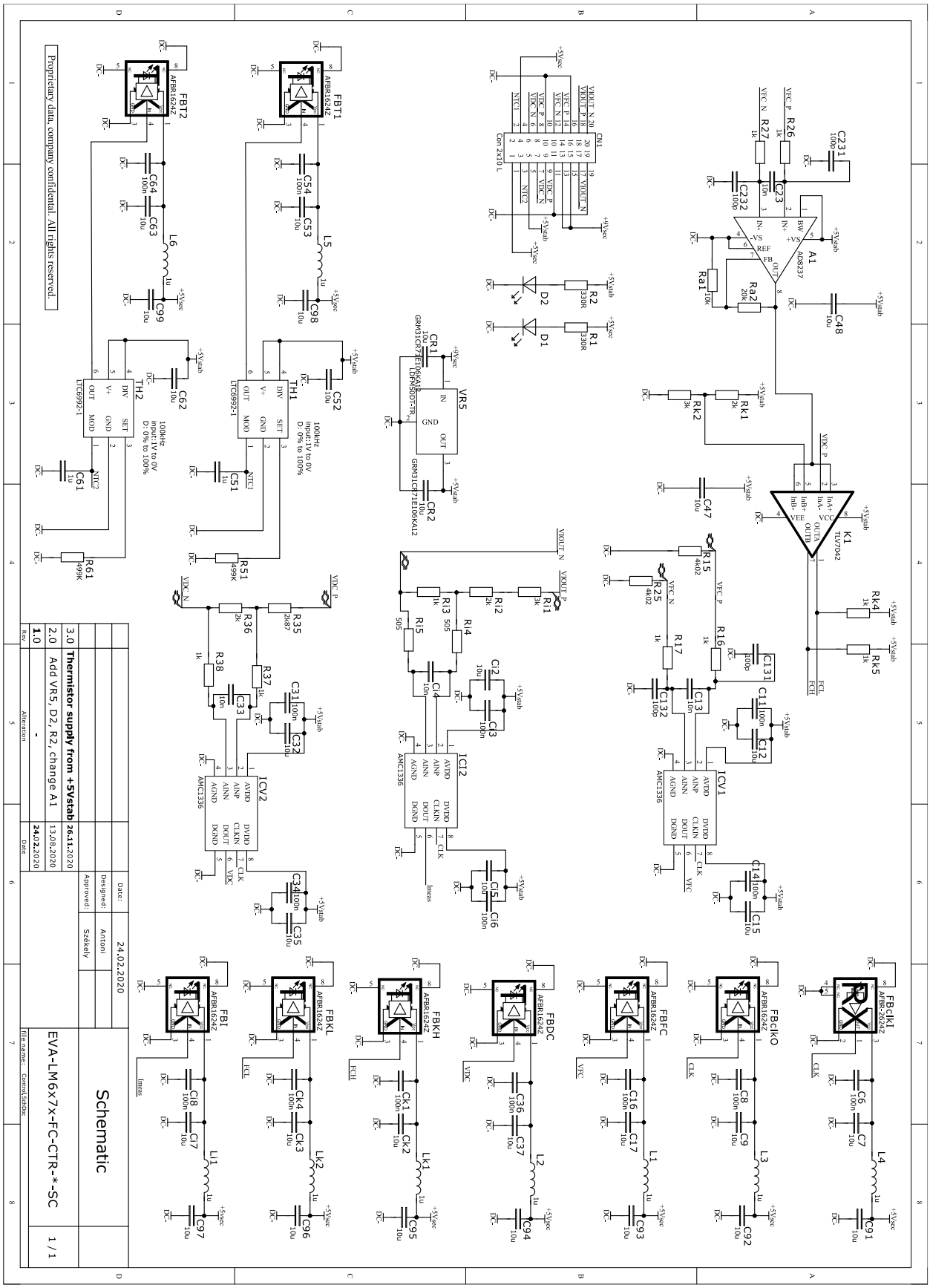
$$P_{in_{inv}} = P_{loss_{inv}} + P_{out} = 43062{,}31\,W$$

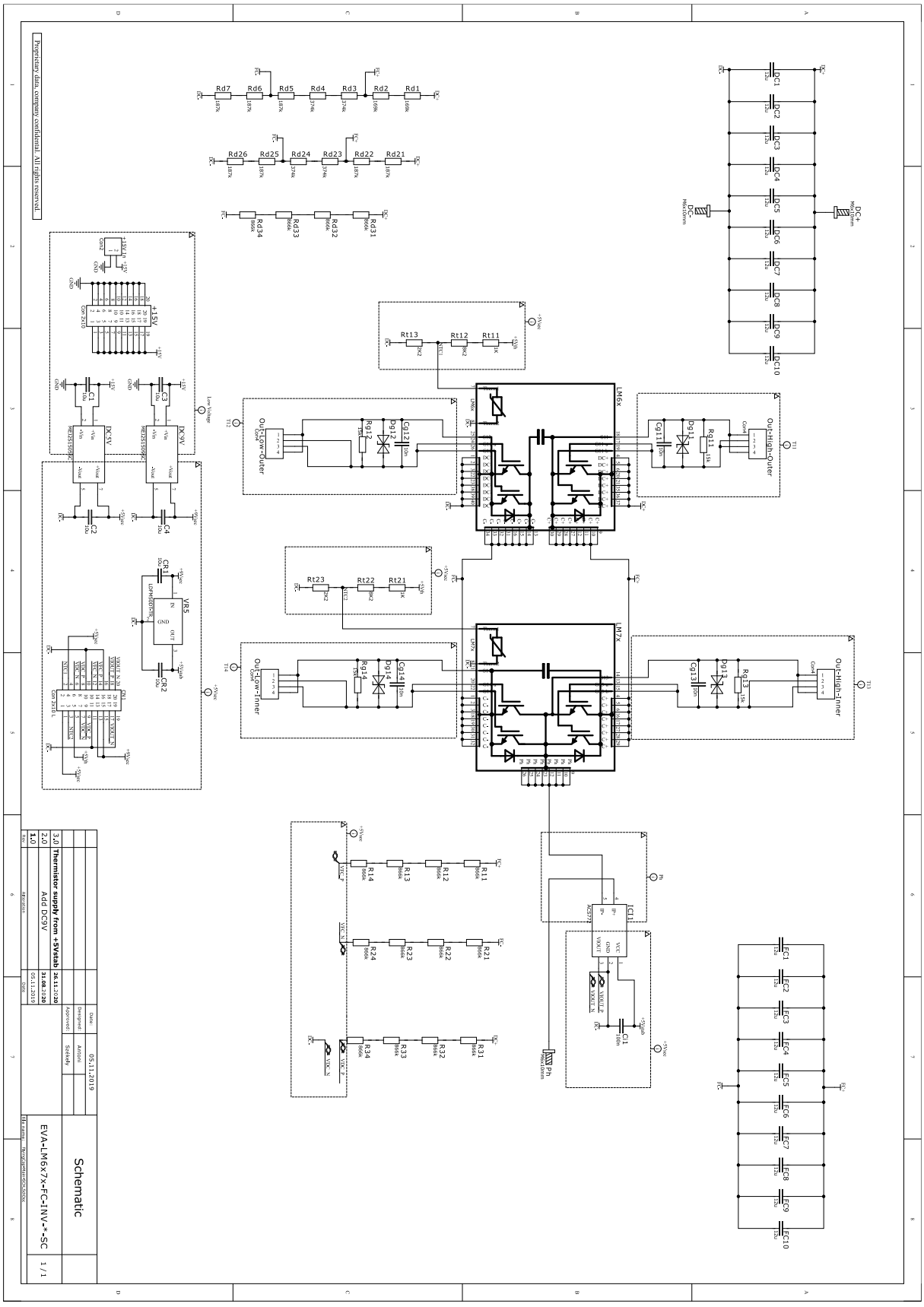
$$\eta_{inv} = \frac{P_{out}}{P_{in_{inv}}} \cdot 100\% = \frac{42143{,}56\,W}{43062{,}31\,W} \cdot 100\% = 97{,}88\,\%$$

7 Fabrication documents

7.1 Schematics


Proprietary data, company confidential. All rights reserved.
Schematic
EVA-LM6x7x-FC-DRV-*-SC
1 / 1
05.11.2019
Antoni
Székely
2.0
Change R11-R16, D11-D14, DRV
In
Out
DC1
DRV
VR5
HB1
HB2
FB
L1
R1
R2
R3
R4
R11
R12
R13
R14
R15
R16
Rgon
Rgoff
D1
DZ1
D11
D12
D13
D14
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
Low Voltage


Proprietary data, company confidental. All rights reserved.
Schematic
EVA-LM6x7x-FC-CTR-*-SC
file name: Control_Sch.Doc
1 / 1
Rev.
Alteration
Date
1.0
-
24.02.2020
2.0
Add VR5, D2, R2, change A1
13.08.2020
3.0
Thermistor supply from +5Vstab
26.11.2020
Approved:
Designed:
Date:
Szekely
Antoni
24.02.2020


Proprietary data, company confidential. All rights reserved.
Schematic
EVA-LM6x7x-FC-INV-**-SC
1 / 1
Add DC9V
Thermistor supply from +5Vstab
31.08.2020
26.11.2020
05.11.2019
Rd7 Rd6 Rd5 Rd4 Rd3 Rd2 Rd1
Rd26 Rd25 Rd24 Rd23 Rd22 Rd21
Rd34 Rd33 Rd32 Rd31
DC1 DC2 DC3 DC4 DC5 DC6 DC7 DC8 DC9 DC10
Rt13 Rt12 Rt11
Rt23 Rt22 Rt21
LM6x
LM7x
Out-Low-Outer
Out-High-Outer
Out-Low-Inner
Out-High-Inner
R14 R13 R12 R11
R24 R23 R22 R21
R34 R33 R32 R31
FC1 FC2 FC3 FC4 FC5 FC6 FC7 FC8 FC9 FC10
+15V
+5V
VR5
CI1
C1
C2
C3
C4
C11

7.2 BOM

7.2.1 DRV Card

Nr.	Name	Value	Type	Manufacturer	Designators	Qty.
1	Amplifier	10 µF	GRM31CR71E106KA12	Murata	C11, C12, C14, C15, C19, C20, C21	7
2	Capacitor	1 µF	C0805C105K3RAC	Kemet	C13	1
3	Capacitor	100 nF	0805B104K500CT	Walsin	C16	1
4	Capacitor	1 nF	C0603C102K5RACTU	Kemet	C17	1
5	Capacitor	33 pF	C0603C330J3GACTU	Kemet	C18	1
6	LED		MCL-S270GC	Multicomp	D1	1
7	Diode		1N4148W-E3-08	Vishay	D11, D12, D13, D14	4
8	DC/DC	+15/+15;-5 V	MGJ2D151505SC	Murata	DC1	1
9	IC		UCC27537	Texas Instruments	DRV	1
10	Zener	10 V	BZM55C10	Vishay	DZ1	1
11	Fiber		AFBR-2624Z	Broadcom (former AVAGO)	FB	1
12	MOSFET		IRF9389	Infineon	HB1, HB2	2
13	Connector		826953-2	TE Connectivity	In, Out	2
14	Inductance	1 µH	IMC0805ER1R0J01	Vishay	L1	1
15	Resistor	330 Ω	WR08X3300FTL	Walsin	R1	1
16	Resistor	4,7 kΩ	CRCW08054K70FKEA	Vishay	R2	1
17	Resistor	1 kΩ	WR08X1001FTL	Walsin	R3	1
18	Resistor	8,2 Ω	CRCW08058R20JNEA	Vishay	R4	1
19	Resistor	110 Ω	CRCW0805110RJNEA	Vishay	R11, R12, R14, R16	4
20	Resistor	100 mΩ	ERJ-U6SJR10V	Panasonic	R13, R15	2
21	Resistor	500 mΩ	RCWE1210R510FKEA	Vishay	Rgoff, Rgon	2
22	LDO	5 V	NCP718BSN500T1G	Onsemi	VR5	1

7.2.2 CTR Card

Nr.	Name	Value	Type	Manufacturer	Designators	Qty.
1	Amplifier		AD8237ARMZ	Analog Devices	A1	1
2	Capacitor	100 nF	0805B104K500CT	Walsin	C6, C8, C11, C14, C16, C31, C34, C36, C54, C64, Ci3, Ci6, Ci8, Ck1, Ck4	15
3	Capacitor	10 nF	C1608C0G1H103J080AA	TDK	C13, C23, C33, Ci4	4
4	Capacitor	1 µF	C0805C105K3RAC	Kemet	C51, C61	2

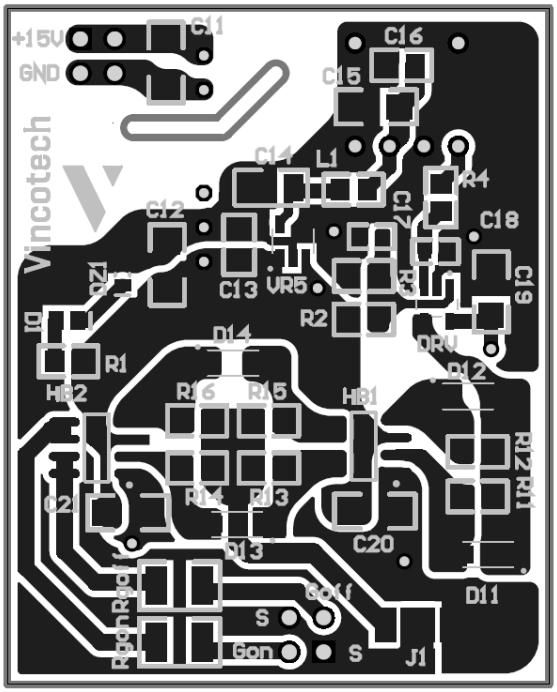
5	Capacitor	100 pF	C0603C101J5GAC7867	Kemet	C131, C132, C231, C232	4
6	Capacitor	10 µF	GRM31CR71E106KA12K	Murata	C7, C9, C12, C15, C17, C32, C35, C37, C47, C48, C52, C53, C62, C63, C91, C92, C93, C94, C95, C96, C97, C98, C99, Ci2, Ci5, Ci7, Ck2, Ck3, CR1, CR2	30
7	Connector		1-826634-0	Tyco	CN1	1
8	LED		MCL-S270GC	Multicomp	D1, D2	2
9	Fiber		AFBR-2624Z	Broadcom (former AVAGO)	FBclkI	1
10	Fiber		AFBR-1624Z	Broadcom (former AVAGO)	FBclkO, FBDC, FBFC, FBI, FBKH, FBKL, FBT1, FBT2	8
11	A/D		AMC1336DWVR	Texas Instruments	ICI2, ICV1, ICV2	3
12	Comparator		TLV7042DGKR	Texas Instruments	K1	1
13	Inductance	1 µH	IMC0805ER1R0J01	Vishay	L1, L2, L3, L4, L5, L6, Li1, Lk1, Lk2	9
14	Resistor	330	WR08X3300FTL	Walsin	R1, R2	2
15	Resistor	4,02 kΩ	CRCW08054K02FKEAC	Vishay	R15, R25	2
16	Resistor	1 kΩ	WR08X1001FTL	Walsin	R16, R17, R26, R27, R37, R38, Ri3, Rk4, Rk5	9
17	Resistor	2,87 kΩ	CRCW08052K87FKEA	Vishay	R35	1
18	Resistor	2 kΩ	CRCW08052K00FKEAC	Vishay	R36, Ri2, Rk1	3
19	Resistor	499 kΩ	CRCW0805499KFKEA	Vishay	R51, R61	2
20	Resistor	10 kΩ	CRCW060310K0FKEA	Vishay	Ra1	1
21	Resistor	20 kΩ	CRCW060320K0FKEA	Vishay	Ra2	1
22	Resistor	3 kΩ	CRCW08053K00FKEAC	Vishay	Ri1, Rk2	2
23	Resistor	505	RT0603BRD07505RL	Yageo-(Phycomp)	Ri4, Ri5	2
24	VCO		LTC6992-1	Linear Technology	TH1, TH2	2
25	LDO	5 V	LDFM50DT-TR	ST Microelectronics	VR5	1
26	PCB		EVA-LM6x7x-FC-CTR-03-PCB			1

7.2.3 INV Card

Nr.	Name	Value	Type	Manufacturer	Designators	Qty.
1	Connector		1-826632-0	TE Connectivity	+15V	1
2	Connector		MCV 1,5/ 2-G-3,81	Phoenix Contact	+15V In	1
3	Capacitor	10 µF	GRM31CR71E106KA12K	Murata	C1, C2, C3, C4, CR1, CR2	6
4	Capacitor	100 nF	0805B104K500CT	Walsin	Ci1	1
5	Capacitor	12 µF	C4AQSBW5120A3LJ	Kemet	DC1, DC2, DC3, DC4, DC5, DC6, DC7, DC8, DC9, DC10, FC1, FC2, FC3, FC4, FC5, FC6, FC7, FC8, FC9, FC10	20
6	DC/DC	+15/+5 V	MEJ2S1505SC	Murata	DC5V	1
7	DC/DC	+15/+9 V	MEJ2S1509SC	Murata	DC9V	1
8	Connector		7461098	Würth Electronik	DC-, DC+, Ph	3
9	Diode		VLIN1616-02G-E3-08	Vishay	Dg11, Dg12, Dg13, Dg14	4
10	Current sensor		ACS772ECB-200B-PFF-T	Allegro Microsystems	ICI1	1
11	Power module		LM6x	Vincotech	LM6x	1
12	Power module		LM7x	Vincotech	LM7x	1
13	Resistor	866 kΩ	ERJP08F8663V	Panasonic	R11, R12, R13, R14, R21, R22, R23, R24, R31, R32, R33, R34, Rd31, Rd32, Rd33, Rd34	16
14	Resistor	169 kΩ	KTR18EZPF1693	Rohm	Rd1, Rd2	2
15	Resistor	374 kΩ	ERJP08F3743V	Panasonic	Rd3, Rd4, Rd23, Rd24	4
16	Resistor	187 kΩ	CRCW2512187KFKEG	Vishay	Rd5, Rd6, Rd7, Rd21, Rd22, Rd25, Rd26	7
17	Resistor	15 kΩ	CRCW080515K0FKEAHP	Vishay	Rg11, Rg12, Rg13, Rg14	4
18	Resistor	1 kΩ	TNPW08051K00DEEA	Vishay	Rt11, Rt21	2
19	Resistor	8,2 kΩ	CPF0805B8K2E1	TE Connectivity	Rt12, Rt22	2
20	Resistor	2,2 kΩ	TNPW08052K20BEEA	Vishay	Rt13, Rt23	2
21	LDO	5 V	LDFM50DT-TR	ST Microelectronics	VR5	1
22	PCB		EVA-LM6x7x-FC-INV-03-PCB			1

7.3 PCB drawings

7.3.1 DRV card



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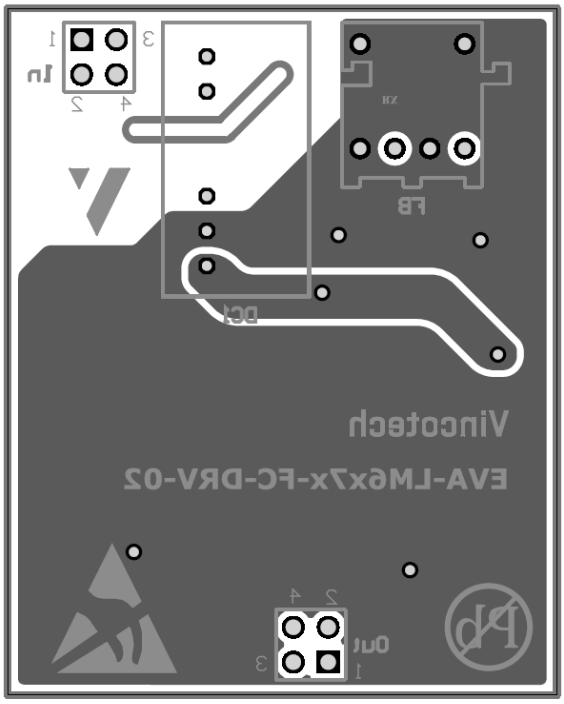
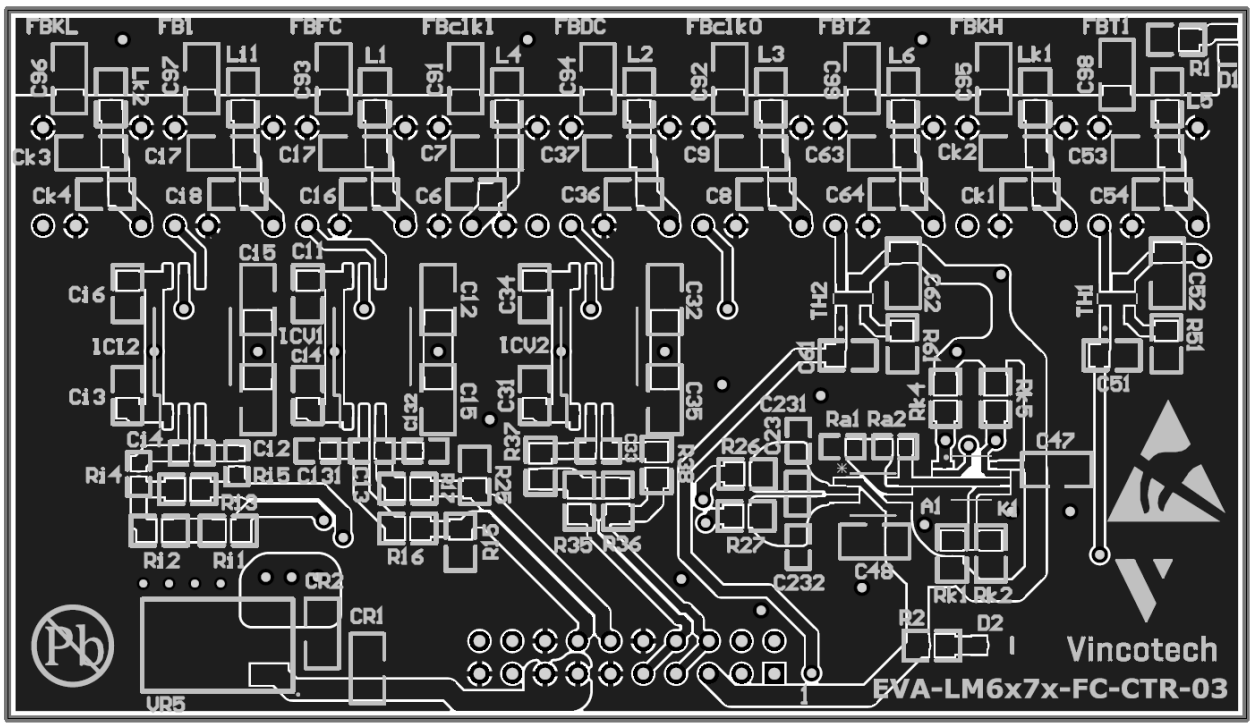


Bottom Layer

7.3.2 CTR Card



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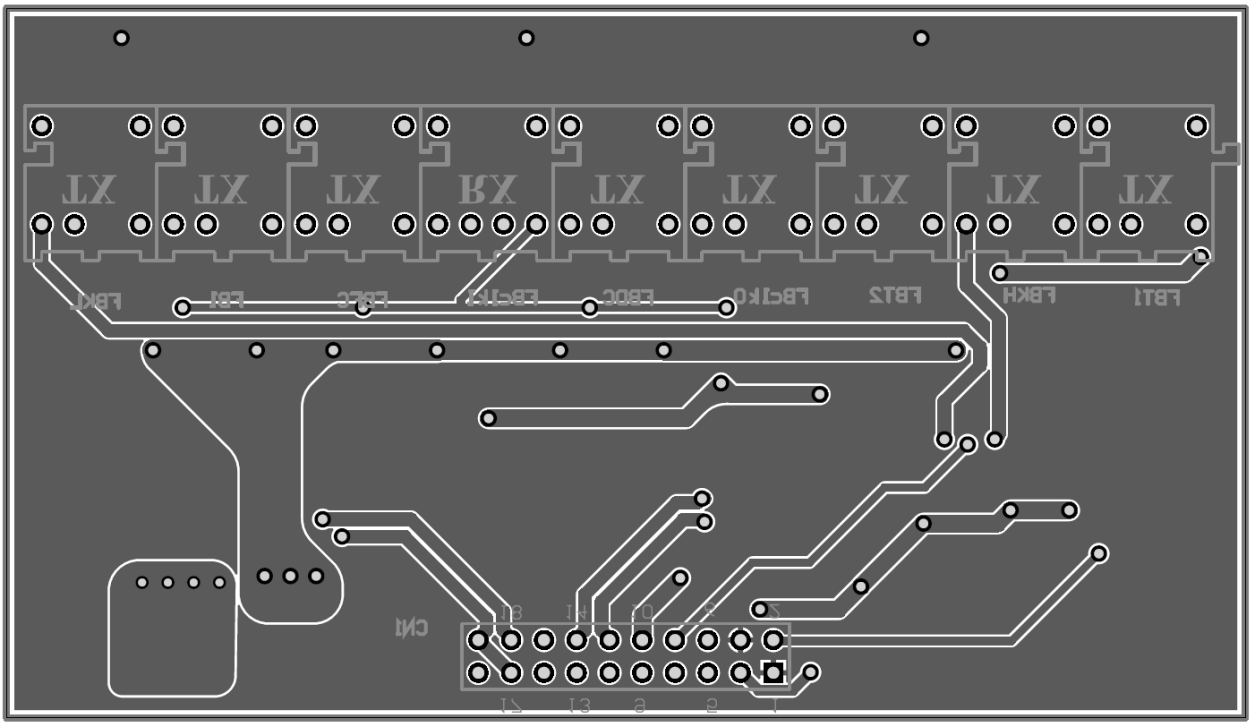
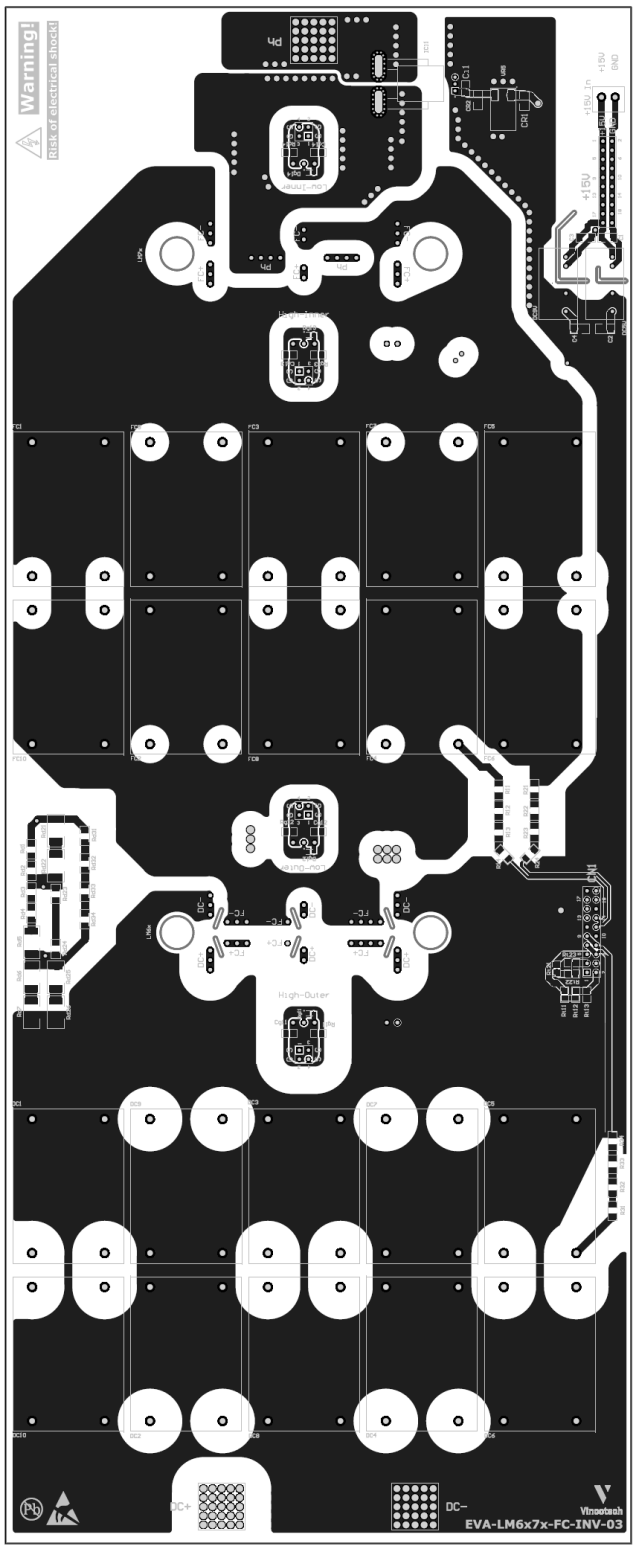


Bottom Layer

7.3.3 INV card



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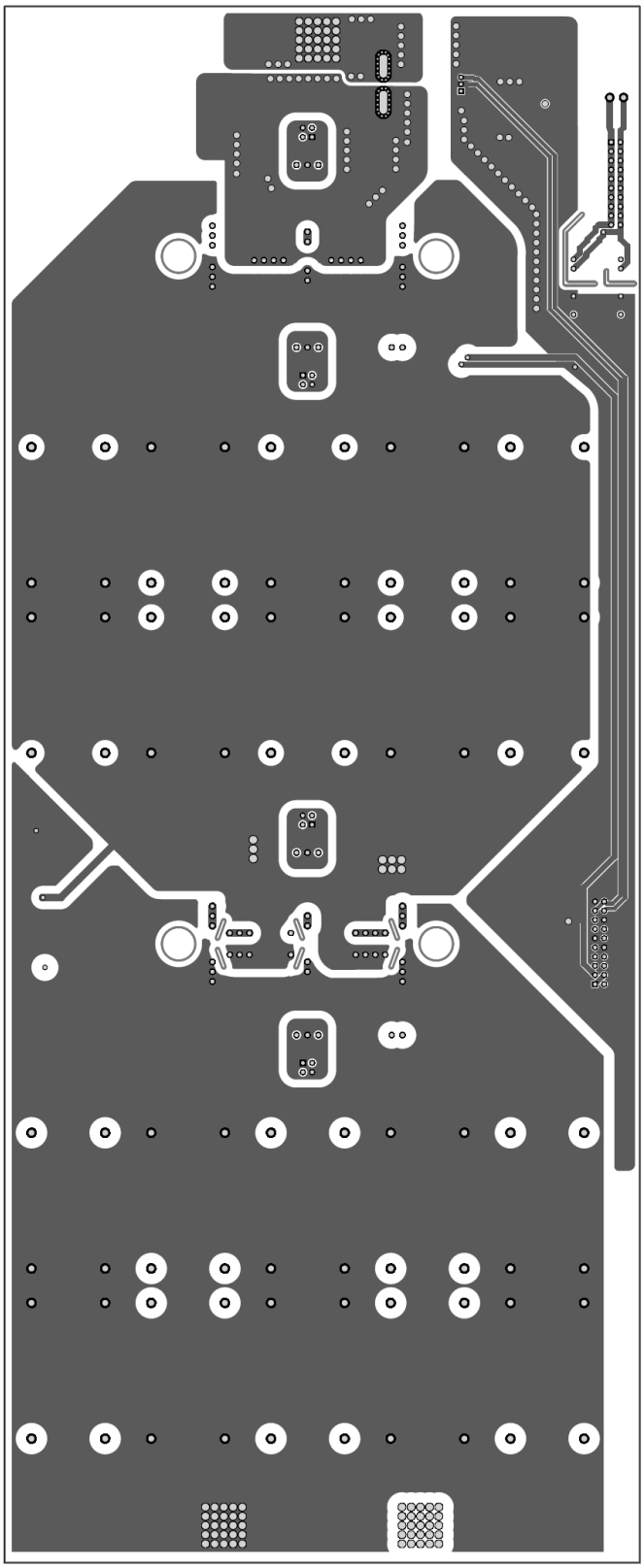

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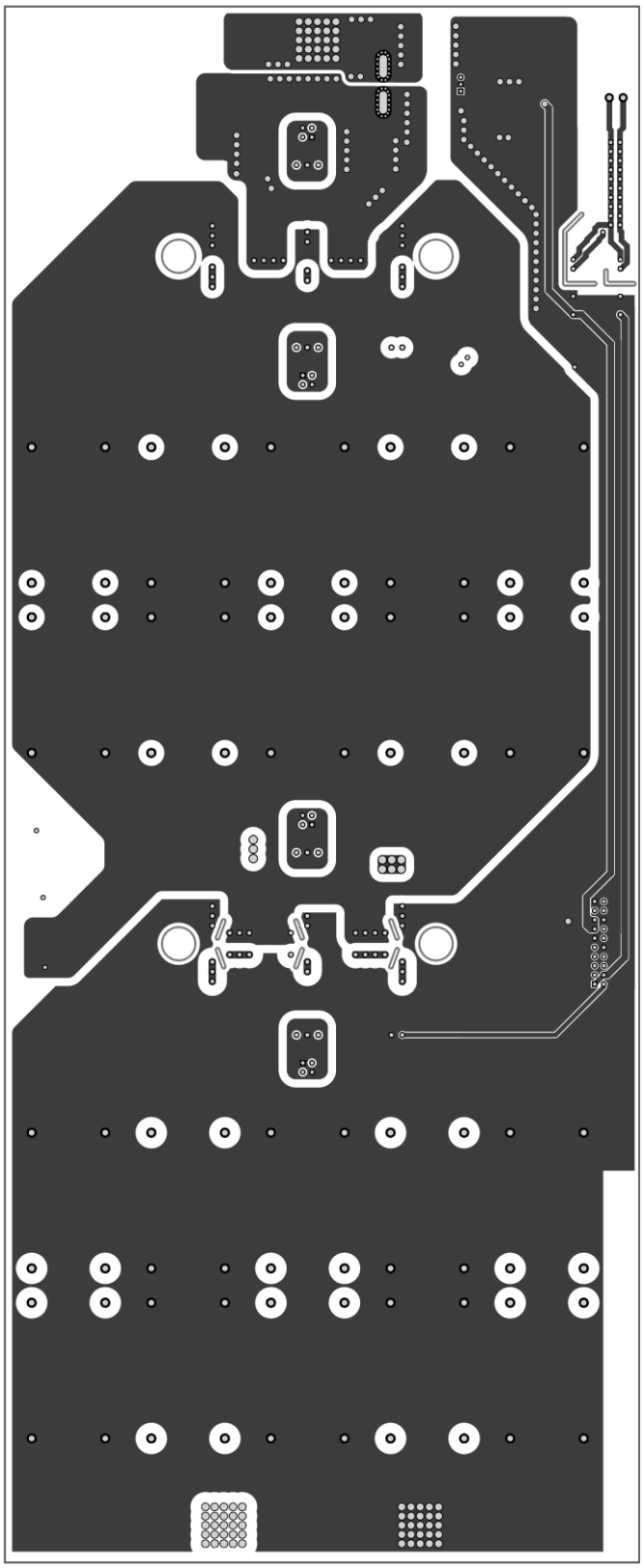

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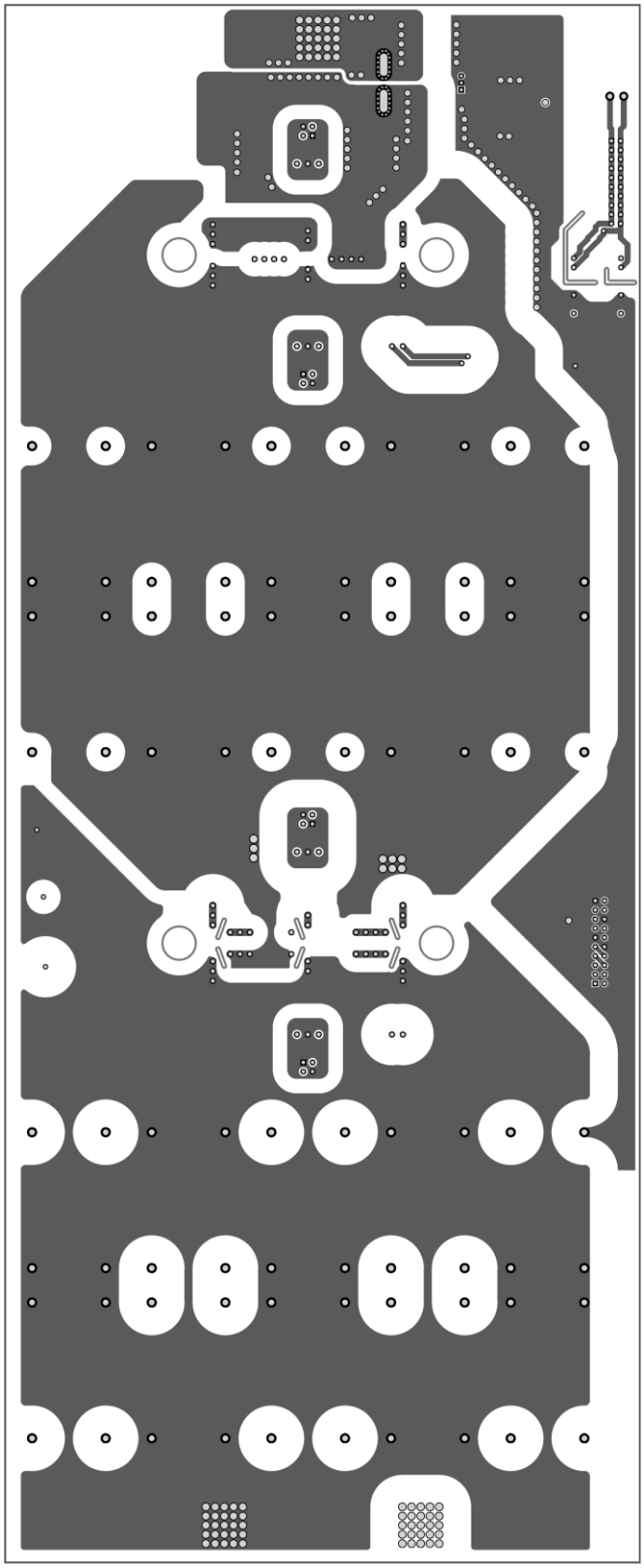

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