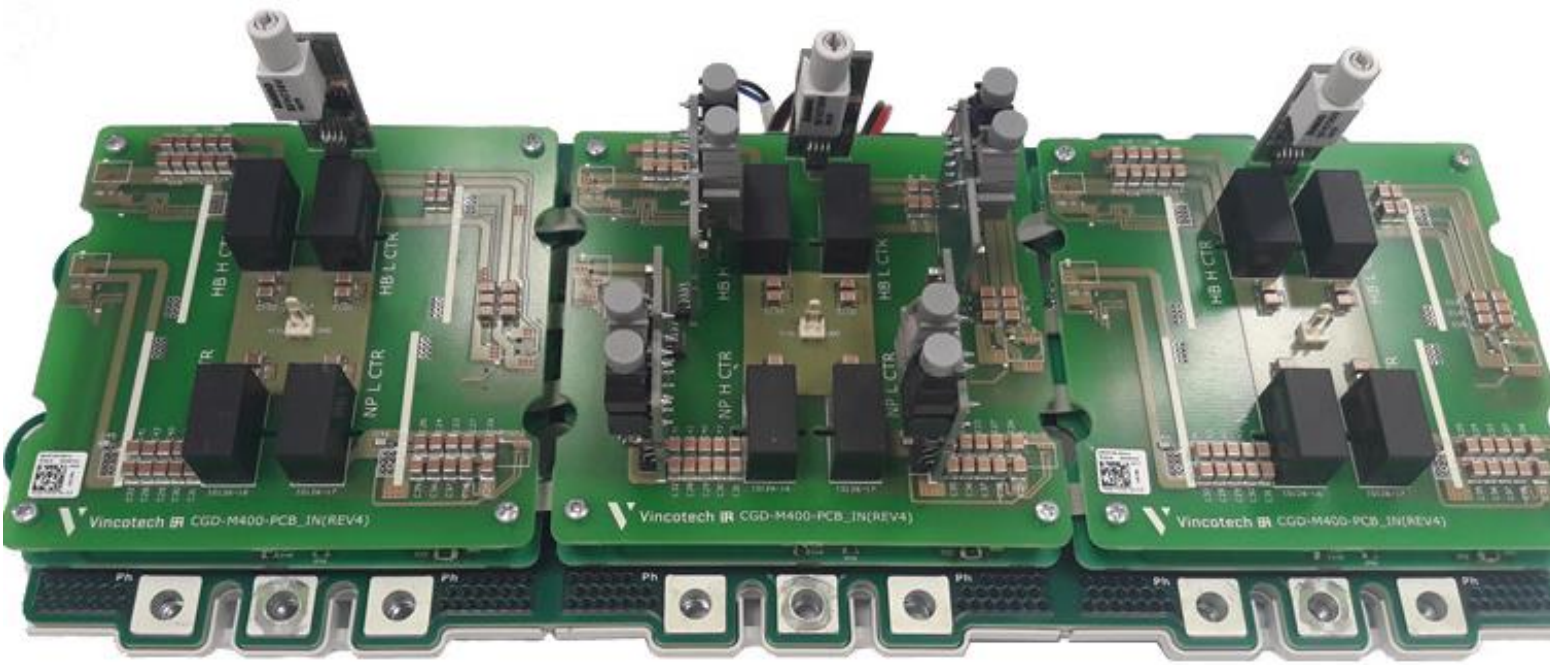
Vincotech

AN for VINcoNPC X12 (LD00FP7X)

How to drive it using the GD-LD00FP7X Vincotech gate driver



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Revision History

Date	Revision Level	Description	Page Number(s)
2018.02.28.	1	First release	32

1 Abstract

This application note describes the gate driver for 70-W624NIA1K8M701-LD00FP70 Vincotech three-level module. The AN will give a short description of the module and a definition of the suitable Vincotech gate driver for this 2400V/1800A NPC (I-Type) power module.

2 Introduction

The 70-W624NIA1K8M701-LD00FP70 is a new member of the Vincotech NPC power modules family VINcoNPC X12 with increased power range. It's a new entrant featuring the VINco X12 housing and a fresh member in the NPC topology. The IGBT M7 and diodes M7 offer a perfect match for the VINcoNPC X12 family. With its power range 2400 V/1800 A targets the 1+ MW 1500 V_{DC} Solar PV Central Inverters, UPS and high speed motor drive market as well. To learn more about Vincotech modules, please visit: www.vincotech.com

3 The power module.

70-W624NIA1K8M701-LD00FP70 is the latest high efficient NPC topology in VINco X12 housing to meet the challenging requirements for central inverters, while retaining the string inverter's speed and flexibility.

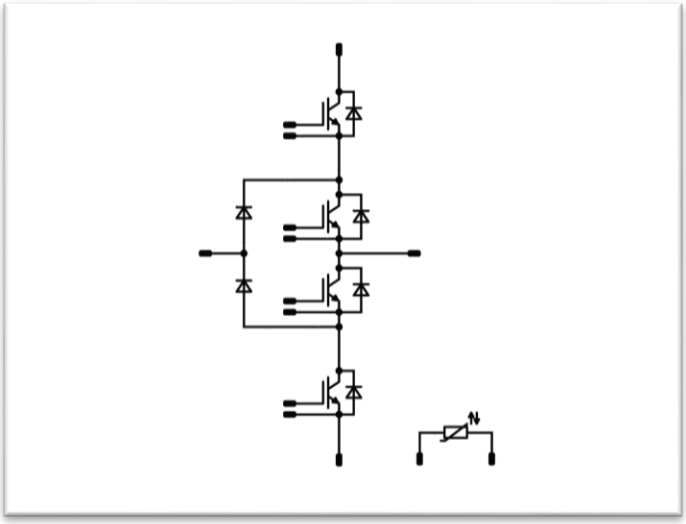

Figure 1: The simplified schematic of the power module

The IGBT M7 and diodes M7 are the perfect match for the VINcoNPC X12 family. M7 dies are up to 25% smaller than those used in the current VINcoNPC X12 for the same current rating, so the nominal current may be stepped up from 1200 A to 1800 A. On top of that, conduction losses are up to 20% lower.

Module main features:

- Optimized connections for three-level topologies
- Low internal inductance (5 nH for low inductive commutation loop; 9 nH for the high inductive loop) enables higher frequencies
- Fully symmetrical layouts for uniform current sharing
- Modular constructions for better thermal performance

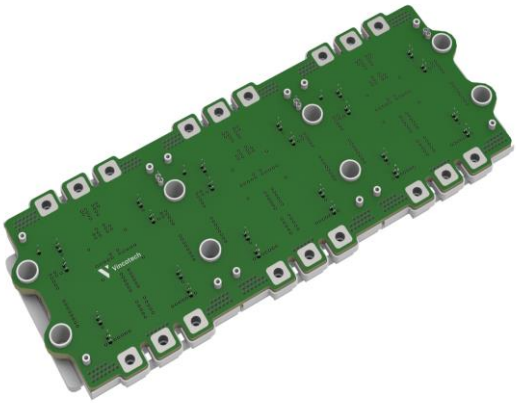

Figure 2: LD0XX in a VINco X12 housing

3.1 Mechanical dimensions, housing

The housing of the LD00 is VINco X12, which can be seen at **figure 3** with its main dimensions. This new housing from power point of view is a triplication of VINco X4 joined together with a common PCB. The input screw connections **DC+**, **GND**, **DC-**, the output screw connections **Ph** are connected together by the power PCB (figure 5), but externally they must be connected together, with a special attention paid for a symmetrical connection to achieve a balanced current sharing.

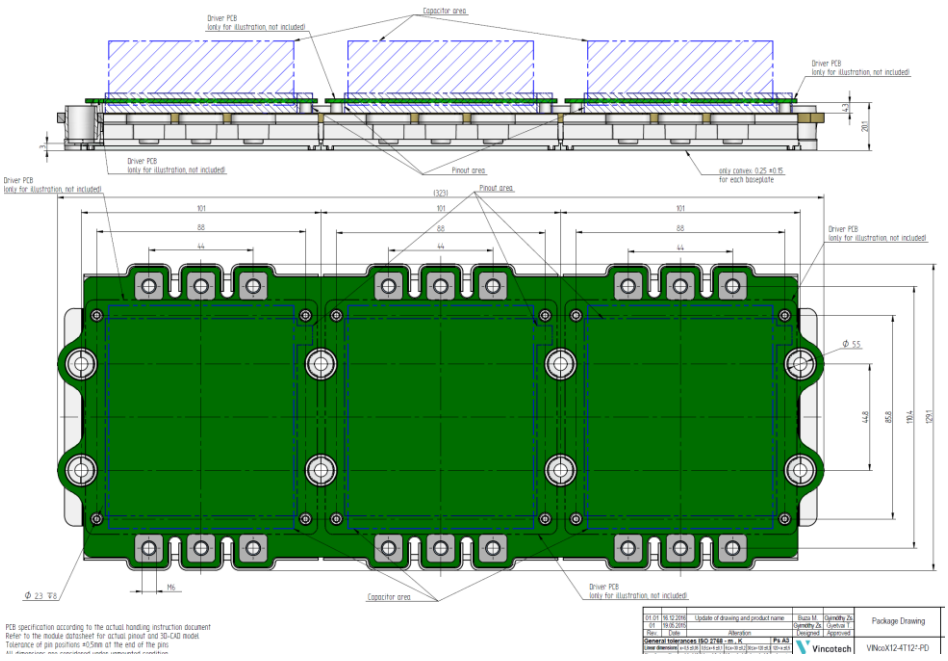

Figure 3: VINco X12

3.2 **Schematic**

The VINcoNPC X12 is a NPC topology realized with a triplication of VINcoNPC X4 in parallel connection. The parallel connection is made by the high power pressed in power PCB, which gives the low stray inductance interconnection. The driver pins are not paralleled by the high power PCB, this one must be made externally by the gate drivers; for more details please refer to the next chapters. The schematic at topology level is shown at **figure 4. Table 1** shows the basic function of each component and their voltage/current ratings.

Figure 5 describes the parallel connection and the pin assignment of the three NPC cells.

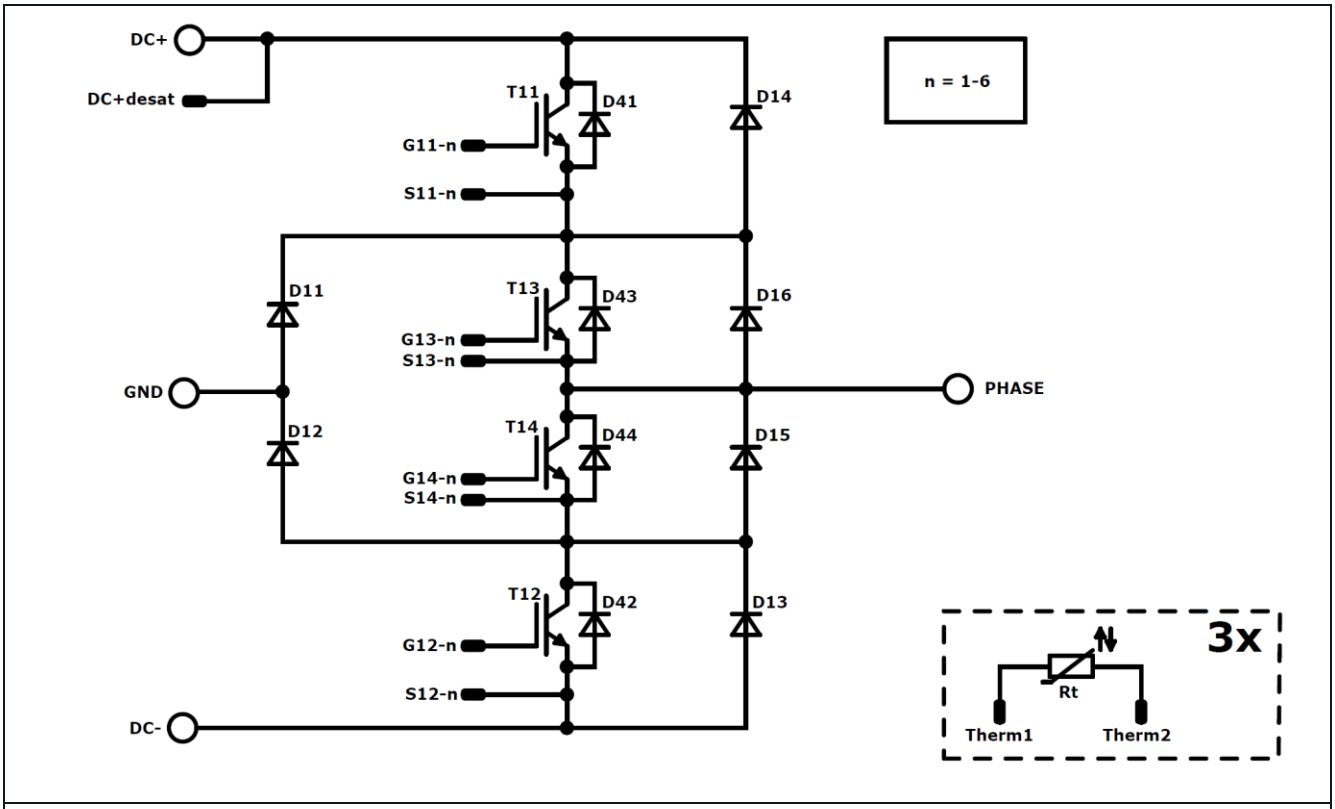

Figure 4: Schematic of the topology

ID	Component	Voltage	Current	Function
T11, T12	IGBT (M7)	1200 V	1800A	Buck IGBT
D11, D12	FWD (M7)	1200 V	1800A	Buck Diode
T13, T14	IGBT (M7)	1200 V	1800A	Boost IGBT
D13, D14	FWD (M7)	1200 V	1800A	Boost Diode
D15, D16	FWD (M7)	1200 V	1800A	Boost IGBT Inv. Diode
D41,D42,D43,D44	FWD	1200 V	90A	IGBT Protection Diode

Table 1: Components , function , voltage /current rating

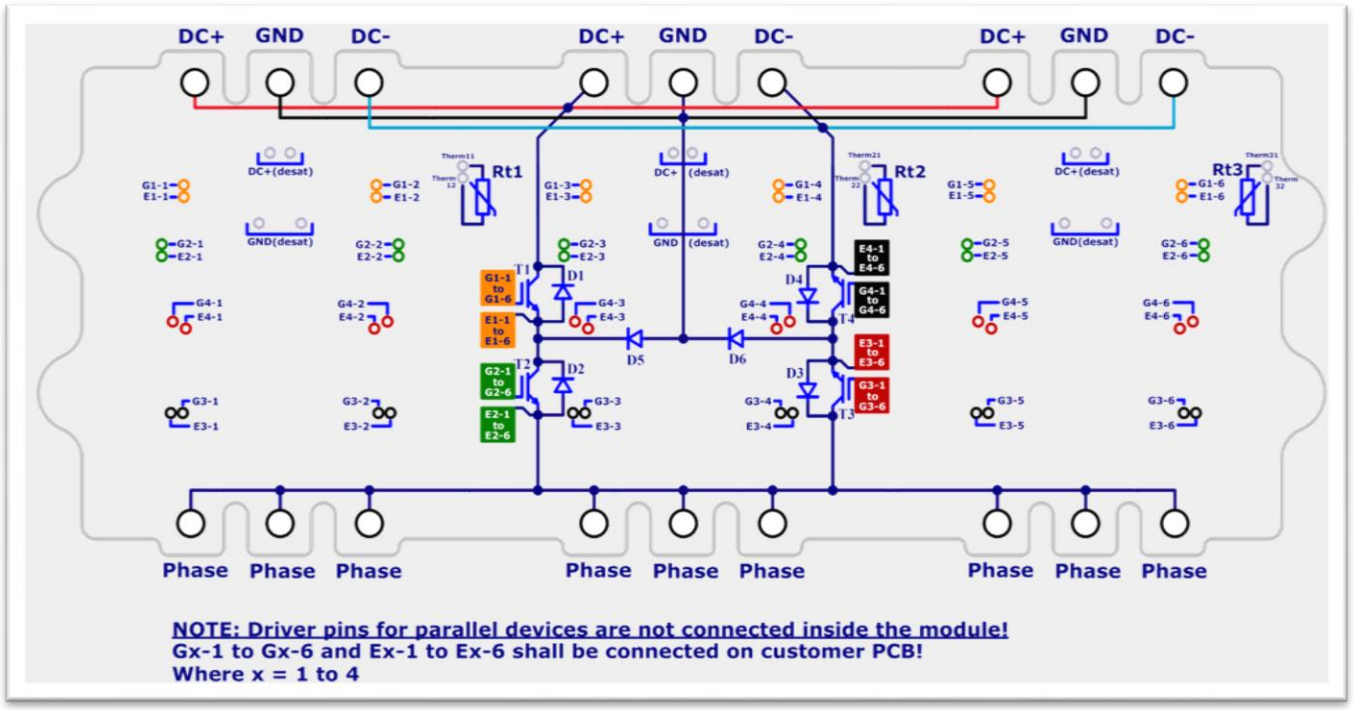

Figure 5: Parallel connection of the 3 NPC cells

4 The gate driver of VINcoNPC X12 (LD00FP7X)

The gate driver of VINcoNPC X12 (LD00FP7X) is based on VINcoNPC X4 (M400) gate driver. VINcoNPC X12 contains three VINcoNPC X4 modules connected in parallel. This structure follows the gate driver design as well. The paralleling of the gate drivers is made in a slave-master-slave configuration. The master gate driver is fully populated with control cards, one control for each channel, while the slave gate driver doesn't include any control cards. The slave gate driver receives the gate signal via the interconnection cables. The static and dynamic current sharing between the three VINcoNPC X4 modules will be guaranteed by module design and gate driver design.

4.1 Signal distribution at S-M-S gate drivers

In order to drive an LD00FP7X power module a SLAVE-MASTER-SLAVE (S-M-S) gate driver configuration will be used. The input PWM signals are received by the CTR cards of the MASTER gate driver. INPUT PWM signals are received via fiber optics, the FAULT signals transition in opposite direction is made in a similar way with fiber optics. Figure 6 shows the block diagram of electrical interconnection of the slave-master-slave gate drivers. The current booster PCB has two current boost stages that are connected in parallel to provide a high gate current when

necessary. Each VINcoNPC X4 module has two gate pins, each for half of the nominal module current. A common gate resistor and separated gate resistors are used for the gates as well, furthermore a common emitter resistor. This way the synchronous switching of the stages can be assured.

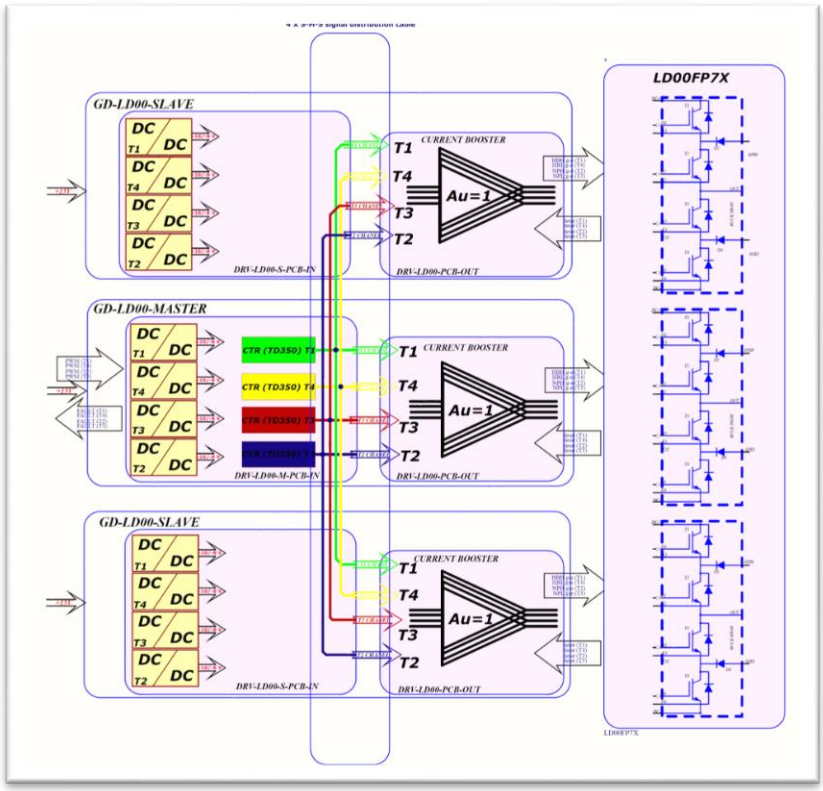

Figure 6: Signal distribution at S-M-S

At figure 7 the parallel connection of the current boosters for one channel is illustrated.

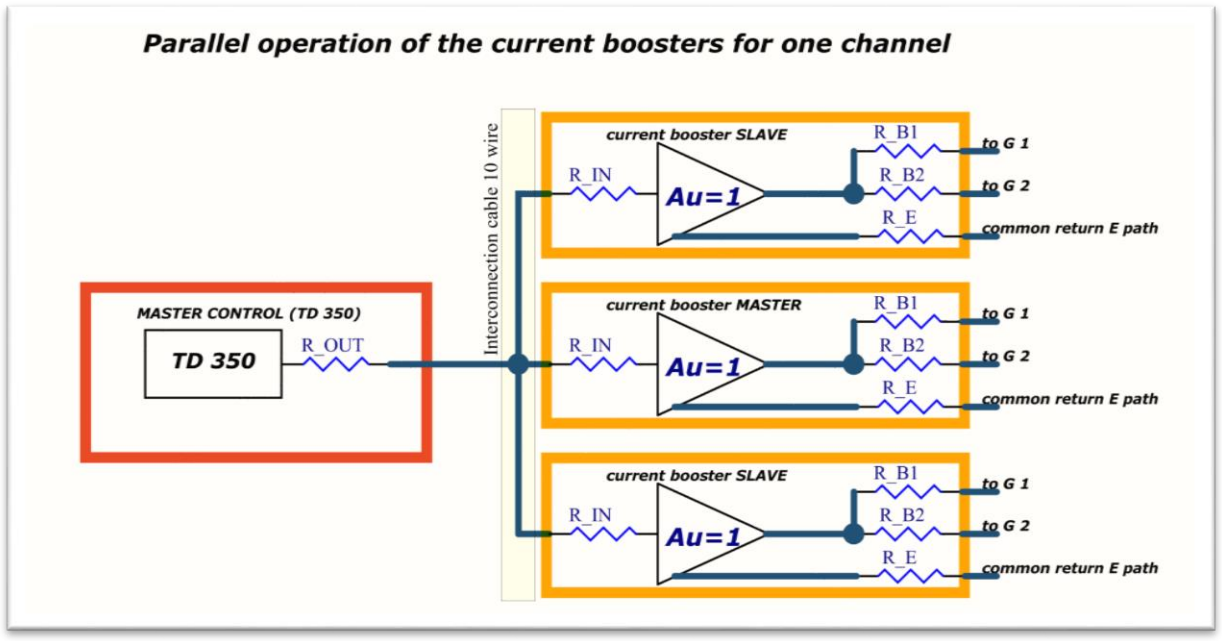

Figure 7: Parallel connection of the current booster

4.2 Mechanical assembly of the gate drivers

LD00FP7X gate driver assembled to the VINcoNPC X12 (LD00FP7X) power module is shown at figure 8. The interconnection between the module and gate driver is made with driver pins which are not connected to the power PCB. These pins are the G-E pins and desaturation detection pin.

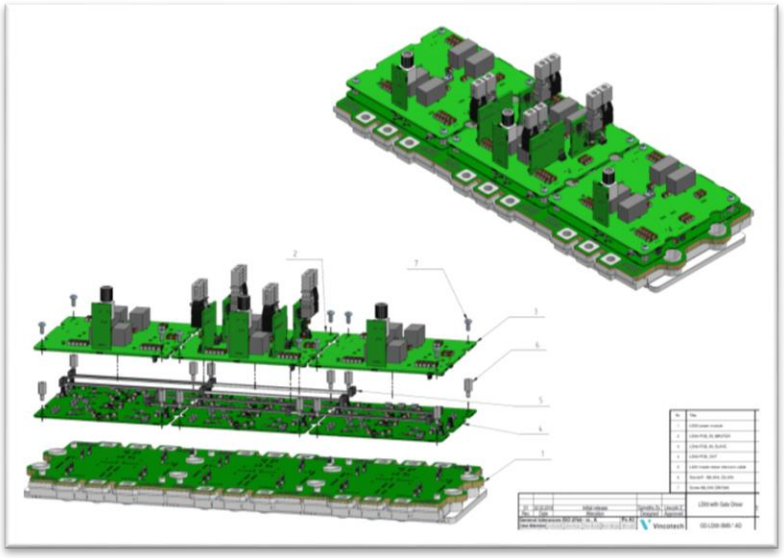

Figure 8: LD00FP7X with S-M-S gate driver

Interconnection of the gate drivers from bottom view:

Figure 9: S-M-S interconnection at IN PCB level

4.3 Interconnection cable for S-M-S operation

Channels: HB H ; HB L ; NP H ; NP L					
Pin	Signal HB H	Signal NP H	Signal NP L	Signal HB L	Comment
1	desat	desat	desat	desat	Desaturation protection
2	+16 V	+16 V	+16 V	+16 V	Positive supply
3	out high	out high	out high	out high	Signal for turn on/off
4	V clamp	V clamp	V clamp	V clamp	Active voltage clamp
5	-8 V	-8 V	-8 V	-8 V	Negative supply
6	clamp	clamp	clamp	clamp	Miller clamping
7	GND	GND	GND	GND	Ground
8	n.c.	n.c.	n.c.	n.c.	not connected

Table 2: Signals on Interconnection cables

The signal distribution between the MASTER and SLAVE-s is assured by 4 interconnection S-M-S cables, 10 wires each. Although the DC/DC converters are paralleled (16V, GND, -8V) - to assure if one DC/DC converter is fed, not only the supplied gate driver is functional, also the others are powered up as well - it is very important that gate drivers are externally supplied by +15V at P17 to avoid the overload of the DC/DC converters of IN-PCB card. All the signals between MASTER and SLAVE are connected in parallel, except the NTC signal – please refer to table 2. The NTC temperature is measured at VINcoNPC X4 level.

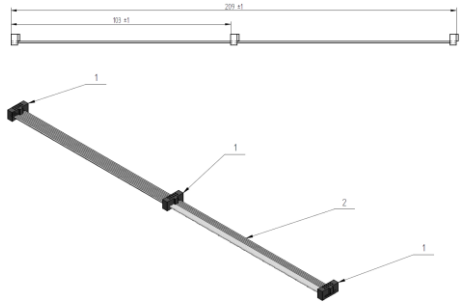

Figure 10: S-M-S interconnection cable

Figure 10 shows the 10 wired interconnection cable. The total length of the cable is 209+/-1 mm, with a symmetrical assembling of the connectors.

5 Features of Driver Board

5.1 Main Features

- Independent drivers for each switch (channel)
- Single 15 V power supply input with 3000VAC isolation
- Gate voltage of -8 V / +16 V
- DC/DC converter / VINcoNPC X4 /channel
- Non-inverting PWM inputs
- Optical Fiber Input and Output signals
- Desaturation protection
- Two level turn-off with 11 V intermediate level
- Active miller clamp
- Under voltage lockout
- Fault output signal (active high) for each switch
- Isolated PWM coded heatsink temperature sense with thermistor on each VINcoNPC X4
- Gate drive current of ±20 A peak / VINcoNPC X4 /channel
- Active voltage clamp
- PCB designed to fulfill the requirements of IEC61800-5-1, pollution degree 2, over voltage category III

5.2 Electrical parameters

	MIN	TYP	MAX	UNIT	Rem.
U_{CE} – max for IGBT/FWD			1200	V	
P_{max} – max output power supply			2	W	for 1 dc/dc converter
U_S – supply voltage for drivers	14,5	15	15,5	V	See note 1
I_S – Input current no load / full load		30/250		mA	for 1 dc/dc converter
Gate drive supply voltage positive	16,5	17	18	V	$14,5V<V_{in(DC/DC)}<15,5V$
Gate drive supply voltage negative	-7	-8,7	-10	V	$14,5V<V_{in(DC/DC)}<15,5V$
Under voltage lockout	14	14,5	15	V	UVLO top threshold
Under voltage lockout	13	14	14,5	V	UVLO bottom threshold
Desaturation protection		7		V	
f_{sw} – switching frequency		8	16	kHz	See note 2
T_a – Ambient temperature	-25		70	°C	
T_{ST} – Storage temperature	-40		85	°C	
Peak Wavelength of fiber optics R/T		660		nm	
Photosensitivity Spectral Range (S = 80% Smax)	600		780	nm	
Gate drive supply isolation voltage			3000	VAC	1 minutes See note 3
For additional information refer to the datasheet of TD350 from ST Note 1: The secondary voltage for the gate drive will change with the same ratio. Note 2: Limitation by IGBT losses Note 3: For conformance with IEC 62109-1 the input supply of the DC-DC converter (15V) should be connected to the inverter neutral potential					
Table 3: Electrical parameters					

5.3 Channel Assignment

Each IGBT has its own CTR (control card) and current booster stage.

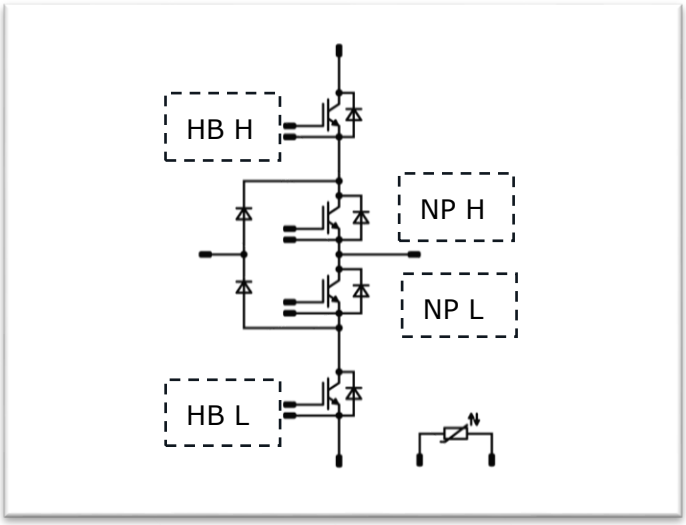

Figure 11: Channel Assignment at schematic level

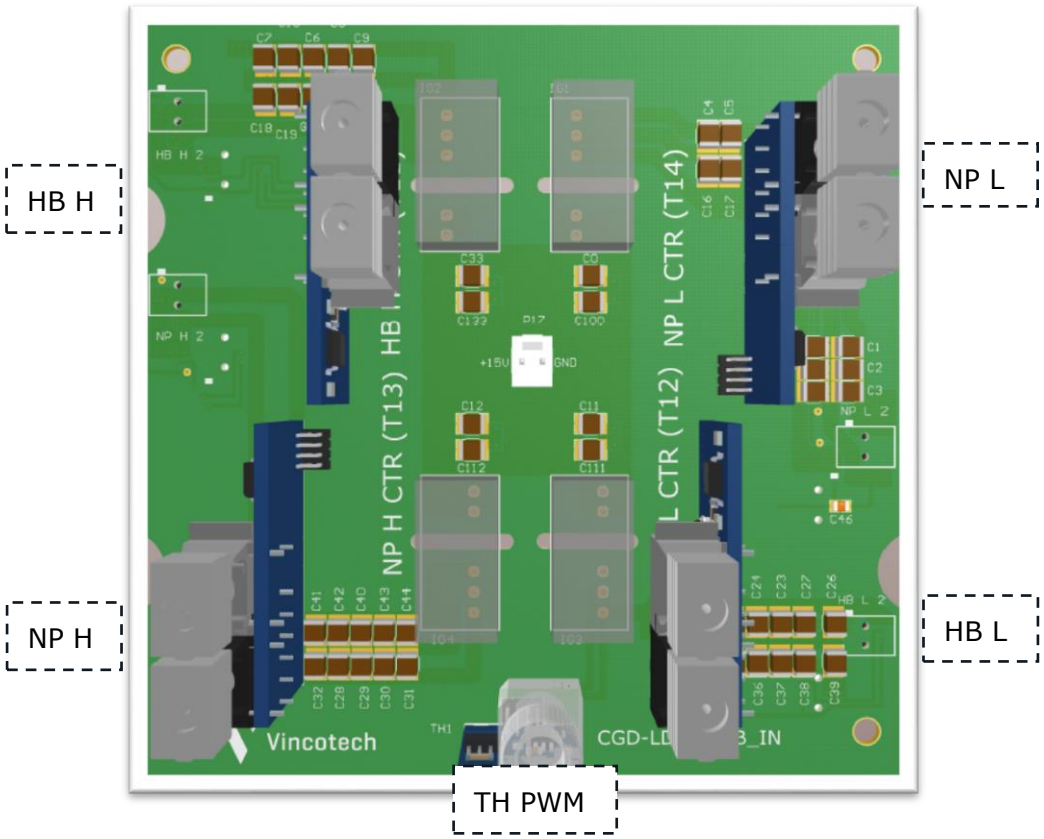

Figure 12: Channel Assignment on IN-PCB

The PWM signal has to be supplied for each CTR card in RX receiver, the FAULT signal of each channel is transmitted by the TX of each CTR card.

The PWM signal of the TH (thermal) card transmitted via SFH756V with polymer optical fiber 2,2mm diameter 650nm. Thermal TH card converts the measured NTC value to 5V PWM signal.

6 Description of Electrical Parts

This chapter describes the different electrical parts like input signals, output signals and driver circuits for a better understanding of the Gate Driver.

6.1 Required power supplies

To ensure a correct operation of the evaluation kit one single +15 V power supply for all gate drivers. The +15 V has to be supported through the connector P17. The +15V at P17 has to be supplied at MASTER and SLAVE as well. The PWM input, FAULT and temperature measurement output are implemented via optical fiber, no additional power supply is required for the CTR cards.

6.2 Input / output signals

Each channel needs its own PWM control signal, dedicated receiver U1 (AFBR2529Z) located on CTR card, which receives this control signal. Each switch has its own fault output activated by under voltage lockout or by desaturation. Fault reported through U2 (AFBR1629Z). The output of the temperature is a PWM signal available on U5 (SFH756) TH-PCB card.

6.3 TH-PCB, temperature measurement

The temperature output is generated with a voltage-controlled pulse width modulator. It is supported to the fiber optic connector U5. The temperature measurement is made in each VINcoNPC X4 module, so in total we have three temperature output signals / VINcoNPC X12. The attached diagram shows the duty cycle as a function of the NTC temperature.

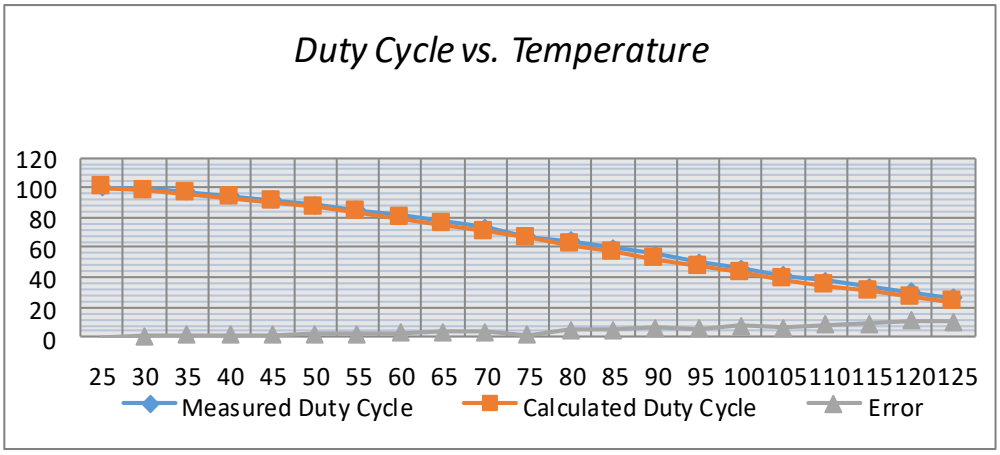

Figure 13: Duty cycle of temperature output

The duty cycle of the PWM signal generated by **LTC6992-1** is directly proportional to the measured module temperature.

An internal +5 V supply is required to power the **LTC6992-1**. The input of the +5 V stabilizer is the +16 V hb L coming from the power supply PCB.

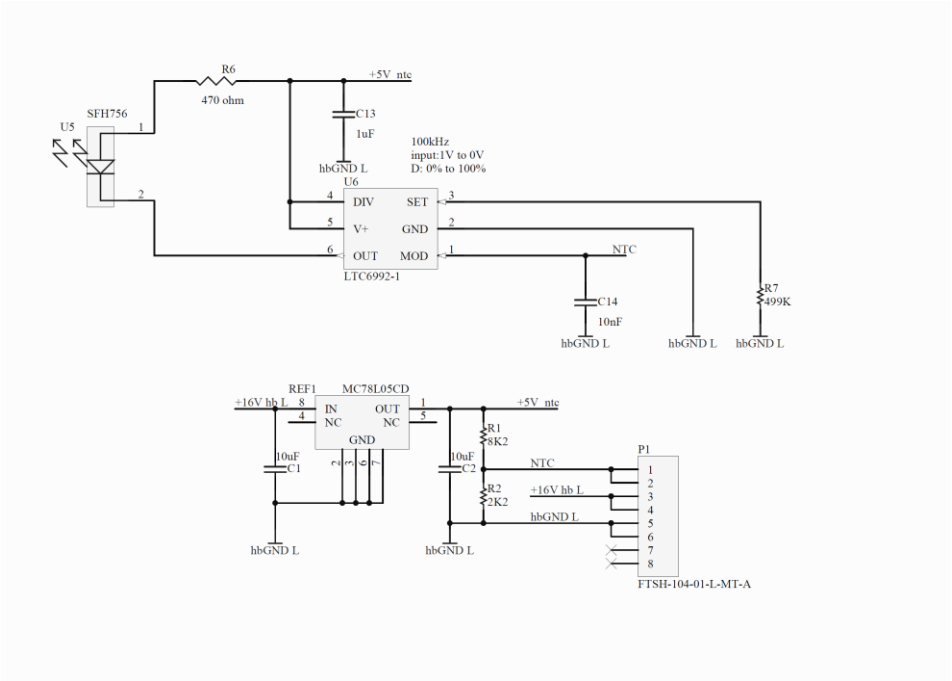

Figure 14: TH-PCB schematic with LTC6992-1 (Voltage-Controlled Pulse Width Modulator)

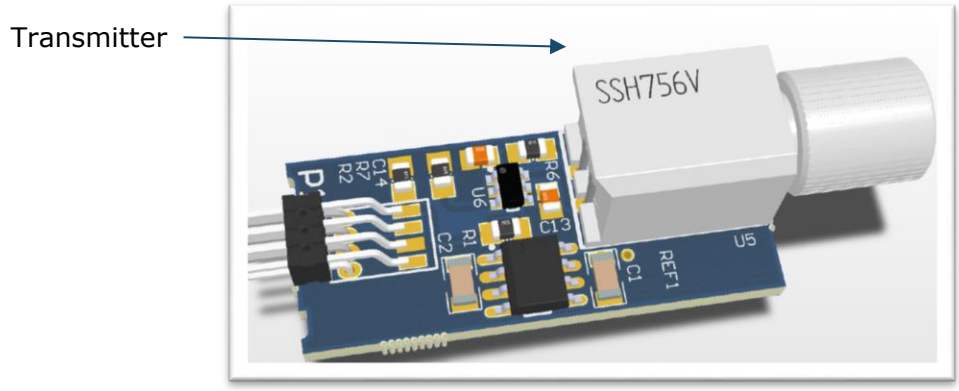

Figure 15: TH-PCB 3D overview

6.4 IN-PCB, dc/dc power supply

Upper PCB called IN-PCB has three main functions

- Supply +15/-8 V asymmetric on/off voltage for each channel.
- Makes possible the SLAVE-MASTER-SLAVE operation, holds the interconnection connectors: fig 16
- Base for the CTR cards (MASTER)

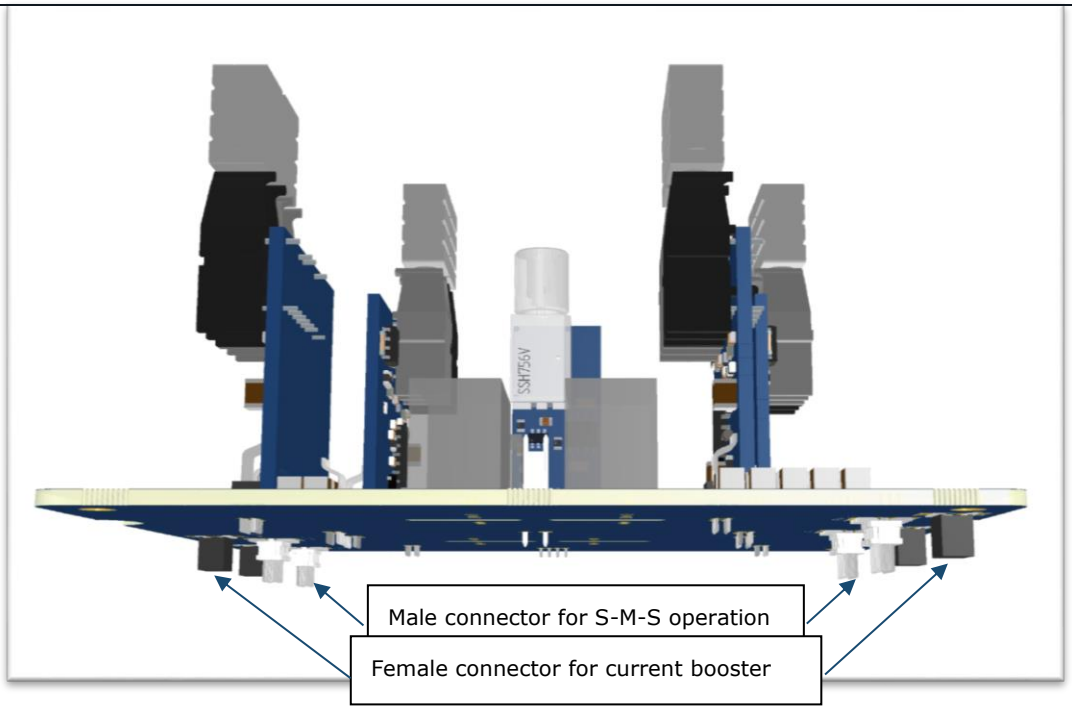

Figure 16: IN-PCB 3D overview

The ON/OFF voltage is supplied by IG136-15, 2W DC/DC converter, with 3000 VACrms isolation voltage. The IN-PCB in case of the MASTER gate driver it is populated with CTR cards while in case of the SLAVE-s there is no CTR-PCB.

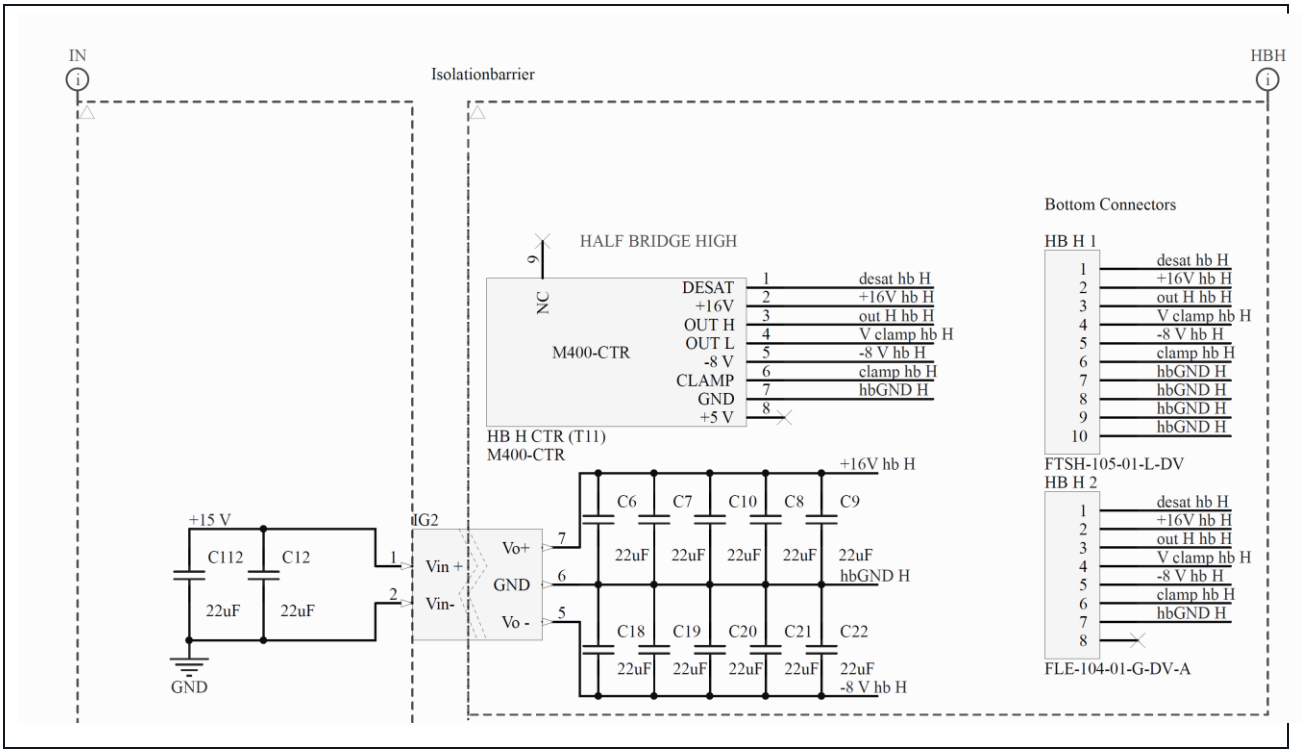

Figure 17: one channel of IN-PCB with CTR card and DC/DC converter.

6.5 CTR-PCB, gate driver IC: TD350

The interface between the control and gate driver is made with fiber optic interconnection. Main components of the CTR card: receiver-AFBR2529Z, fault transmitter-AFBR1629Z, gate driver IC-TD350E, +5V voltage stabilizer, status LED-s

Main features of the IGBT gate driver IC (TD350E)

- Active Miller clamp
- Two-level turn-off with adjustable level and delay
- Desaturation detection
- Fault status output
- Negative gate drive capability
- UVLO protection
- 2 kV ESD protection (HBM)

Active Miller clamp: During turn-off, the gate voltage is monitored and the clamp output is activated when gate voltage goes below 2 V (relative to GND). The clamp voltage is VL+3 V max. for a Miller current up to 500 mA. The clamp is disabled when the IN input is triggered again. The current capability of the clamp output is increased by an external PNP bipolar transistor placed on the current booster PCB (bottom PCB).

Two-level turn-off: The two-level turn-off is used to increase the reliability of the application.

During turn-off, gate voltage can be reduced to a programmable level (set by D14 to an 11 V) in order to reduce the IGBT current (in the event of overcurrent). This action prevents both dangerous overvoltage across the IGBT and RBSOA problems, especially at short-circuit turn-off. The two-level turn-off (Ta) delay is programmable through an external resistor (R48) and capacitor (C51) for accurate timing use the following equation:

$$T_a[\mu s] = 0.7 \bullet R48[k\Omega] \bullet C51\ [nF] \qquad T_a \text{ is set to } 1{,}5\ \mu s$$

Turn-off delay (T_a) is also used to delay the input signal to prevent distortion of input pulse width.

Desaturation detection: When the desat voltage goes higher than 7 V, the output is driven low (with 2-level turn-off). The FAULT output is activated. The FAULT state is exited at the next falling edge of IN input. A programmable blanking time is used to allow enough time for IGBT saturation. The blanking time is made of an internal 250 µA current source and an external capacitor (C39). The high voltage diode blocks the high voltage during IGBT off-state (a standard 1 kV); the 1 kΩ resistor filters parasitic spikes and also protects the DESAT input. During operation, the DESAT capacitor is discharged when TD350 output is low (IGBT off). When the IGBT is turned on, the DESAT capacitor starts charging and desaturation protection is effective after the blanking time (tB)

$$t_s = 7.2[V] * C_{39} / 250[\mu A]$$

When a desaturation event occurs, the fault output is pulled down and TD350 outputs are low (IGBT off) until the IN input signal is released (high level), then activated again (low level). In case of a short circuit event the inner IGBT (NPH, NPL) must be switched off after the outer IGBT-s (HBH, HBL). This sequence is hardware programed with an additional desaturation capacitor placed in IN-PCB at desat pin (only MASTER PCB).

C desat=C39=180pF HBH and HBL channels while for NPH and NPL C desat=C39+47pF

Fault status output: the dedicated output pin of the IC is used to signal a fault event (desaturation, UVLO) to a controller. The fault pin drives direct the U2 fiber transmitter via a red colored LED. When a fault event is detected the red LED will lights up.

***Minimum ON time*:** In order to ensure the proper operation of the 2-level turn-off function, the input ON time (Twin) must be greater than the Twinmin value:

$$T_{winmin}=T_a + 2 \bullet R_{del} \bullet C_{51} = 1.5 + 2*0.5*0.47=2\mu s$$

R_{del} is the internal discharge resistor of TD350E 0.5 kΩ (from the datasheet of TD350E)

Input signals smaller than T_a are ignored. Input signals larger than T_{winmin} are transmitted to the output stage after the T_a delay with minimum width distortion ($\Delta Tw = T_{wout} - T_{win}$).

For an input signal width Twin between T_a and T_{winmin}, the output width T_{wout} is reduced below T_{win} (pulse distortion) and the IGBT could be partially turned on. These input signals should be avoided during normal operation.

For more details : http://www.st.com/web/en/resource/technical/document/datasheet/DM00023850.pdf

Schematic of the CTR-PCB:

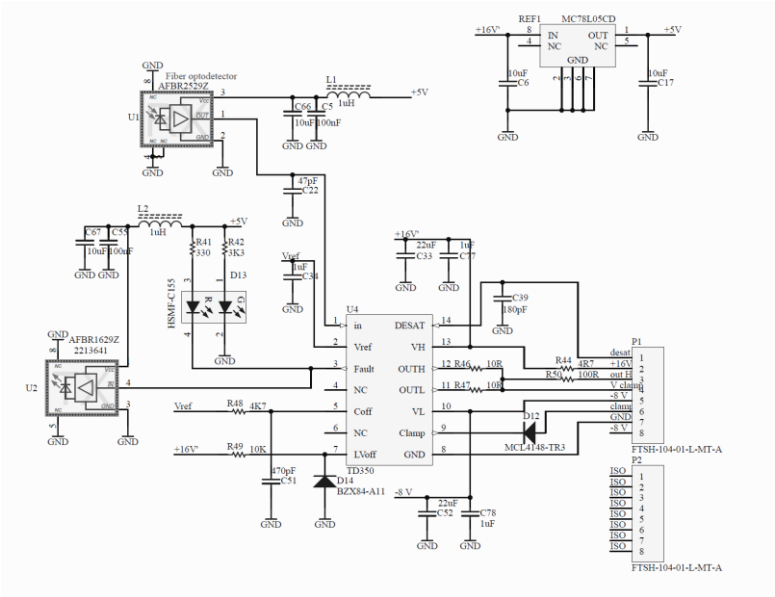

Figure 18: CTR card with TD350E

6.6 OUT-PCB, current booster

Main features of the OUT-PCB

- Current booster +/- 20 A current capability / channel / VINcoNPC X4
- Active miller clamp, additional PNP transistor for clamp current
- Desaturation detection reporting
- Active voltage clamp

Four independent driver channels are assembled on current booster PCB. The MASTER and SLAVE current boosters are the same and they are connected in parallel as shown in previous chapters. Two current boost IC are connected in parallel /channel (ZXGD3006) to provide a high gate current when necessary. A common gate resistor as well as separated gate resistors are used for the gates and the common emitter.

The schematic of one channel is shown in the next figure:

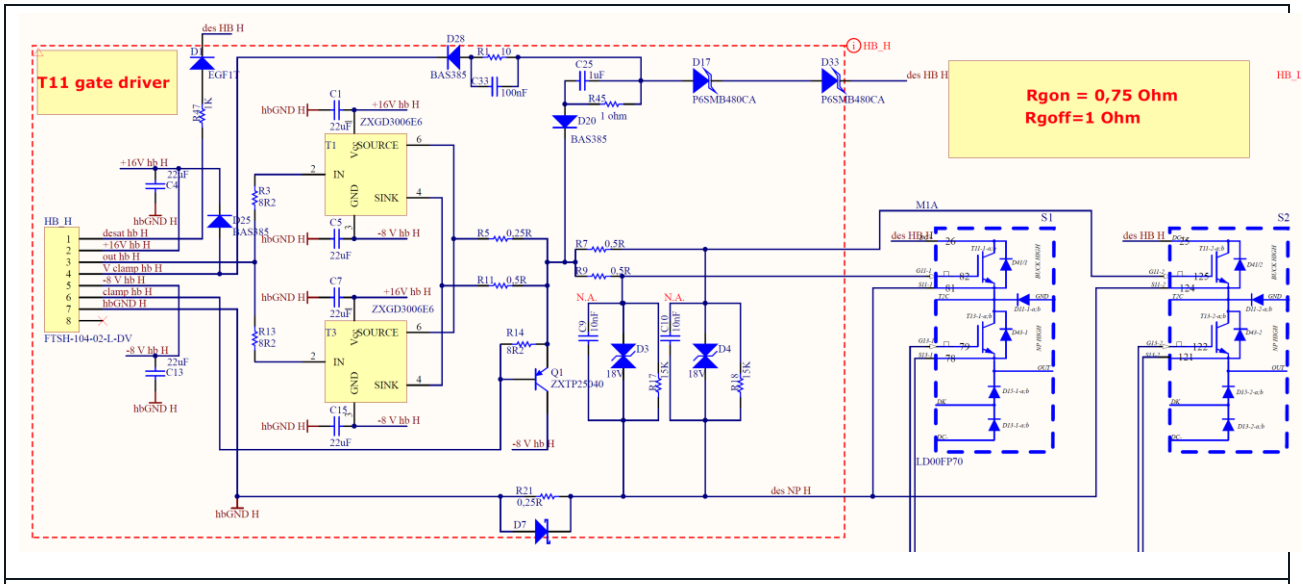

Figure 19: one channel of OUT-PCB

Active voltage clamp:

The rated blocking voltage of the semiconductor switch may never be exceeded. This requirement must be fulfilled under all working conditions including of course turn-off transients from over-current or short –circuit conditions. Due to the unavoidable stray inductances in the layout of the power stage and high values of the current change dI/dt the over voltages in the range of few hundreds volts can be produced. In extreme cases these voltage spikes can take the values higher than the maximal permissible level of the collector-

emitter voltage $V_{CE(max)}$. The zener diodes D33, D17 between collector and gate causes the gate to become turned on when the collector voltage reaches 1200 V

Pin assignment for the male connectors on OUT-PCB

Connector: HB H ; HB L ; NP H ; NP L					
PIN	Chanel HBH	Chanel NPH	Chanel NPL	Chanel HBL	comment
1	desat	desat	desat	desat	Desaturation protection
2	+16 V	+16 V	+16 V	+16 V	Positive supply
3	out high	out high	out high	out high	Signal for turn on/off
4	V clamp	V clamp	V clamp	V clamp	Active voltage clamp
5	-8 V	-8 V	-8 V	-8 V	Negative supply
6	clamp	clamp	clamp	clamp	Miller clamping
7	GND	GND	GND	GND	Ground
8	n.c.	n.c.	n.c.	NTC	not connected / NTC
Table 4: Signals at OUT-PCB					

7 Schematics

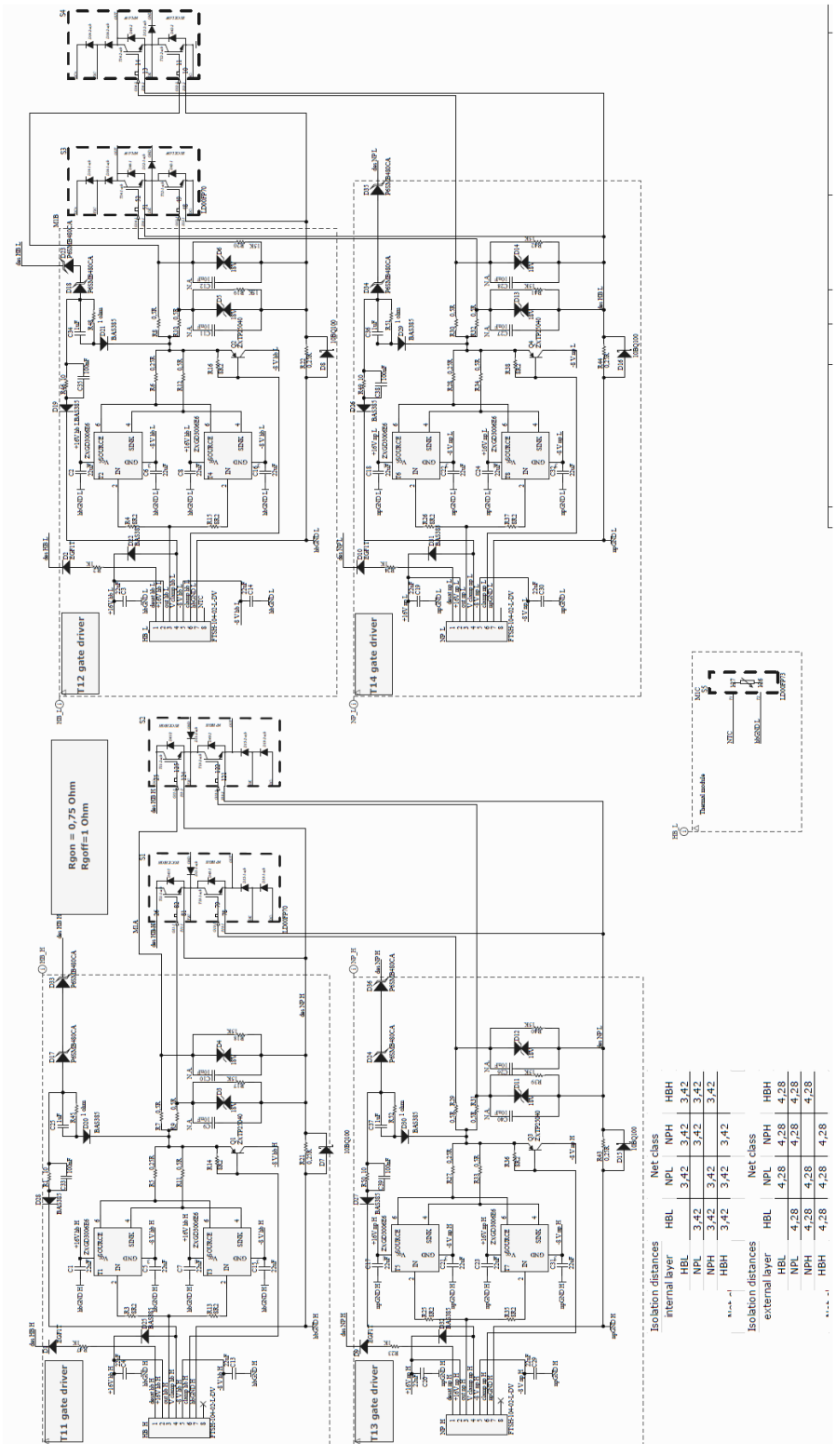

Figure 20: OUT-PCB CURRENT BOOSTER

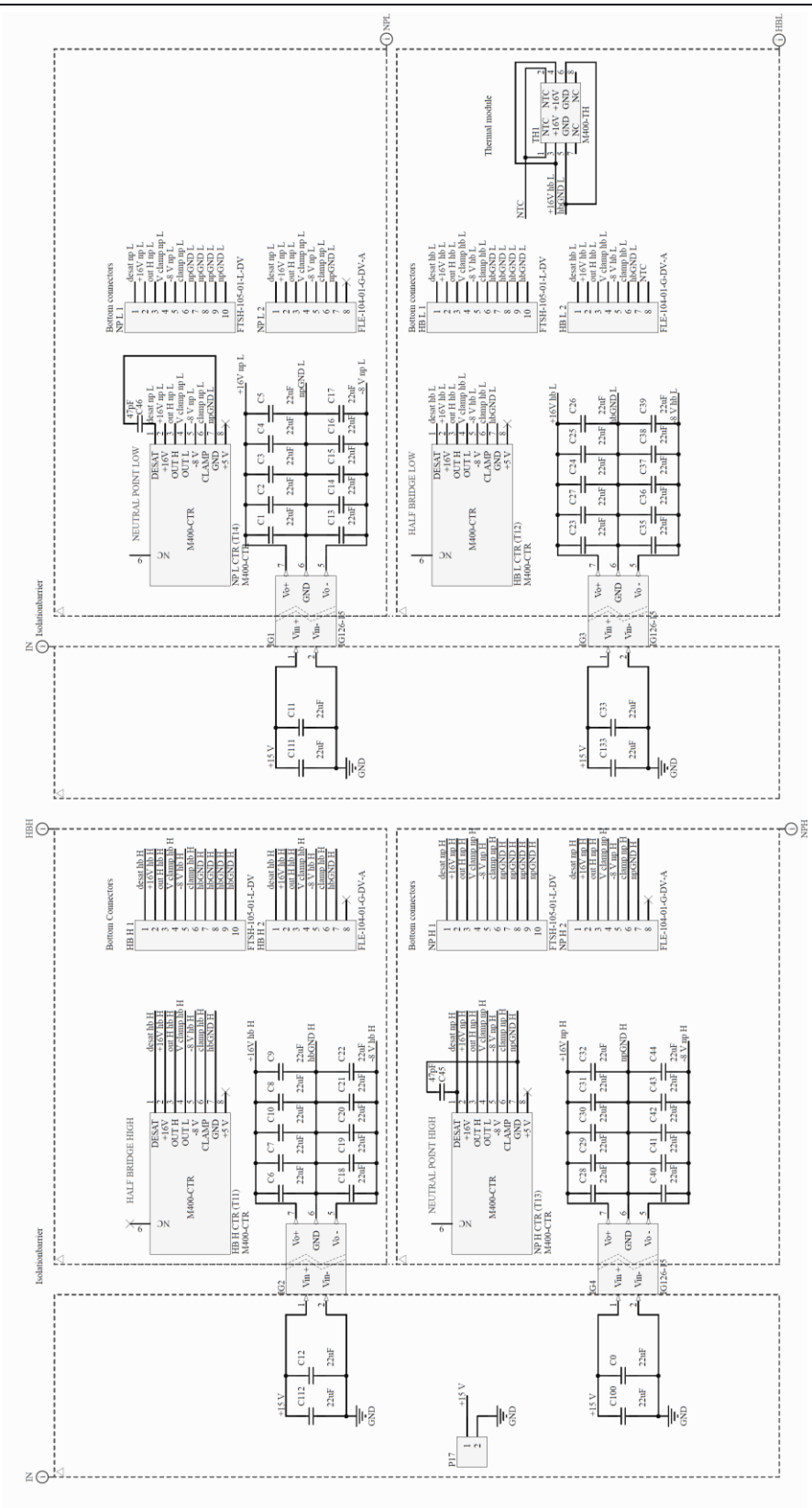

Figure 21: IN-PCB-MASTER

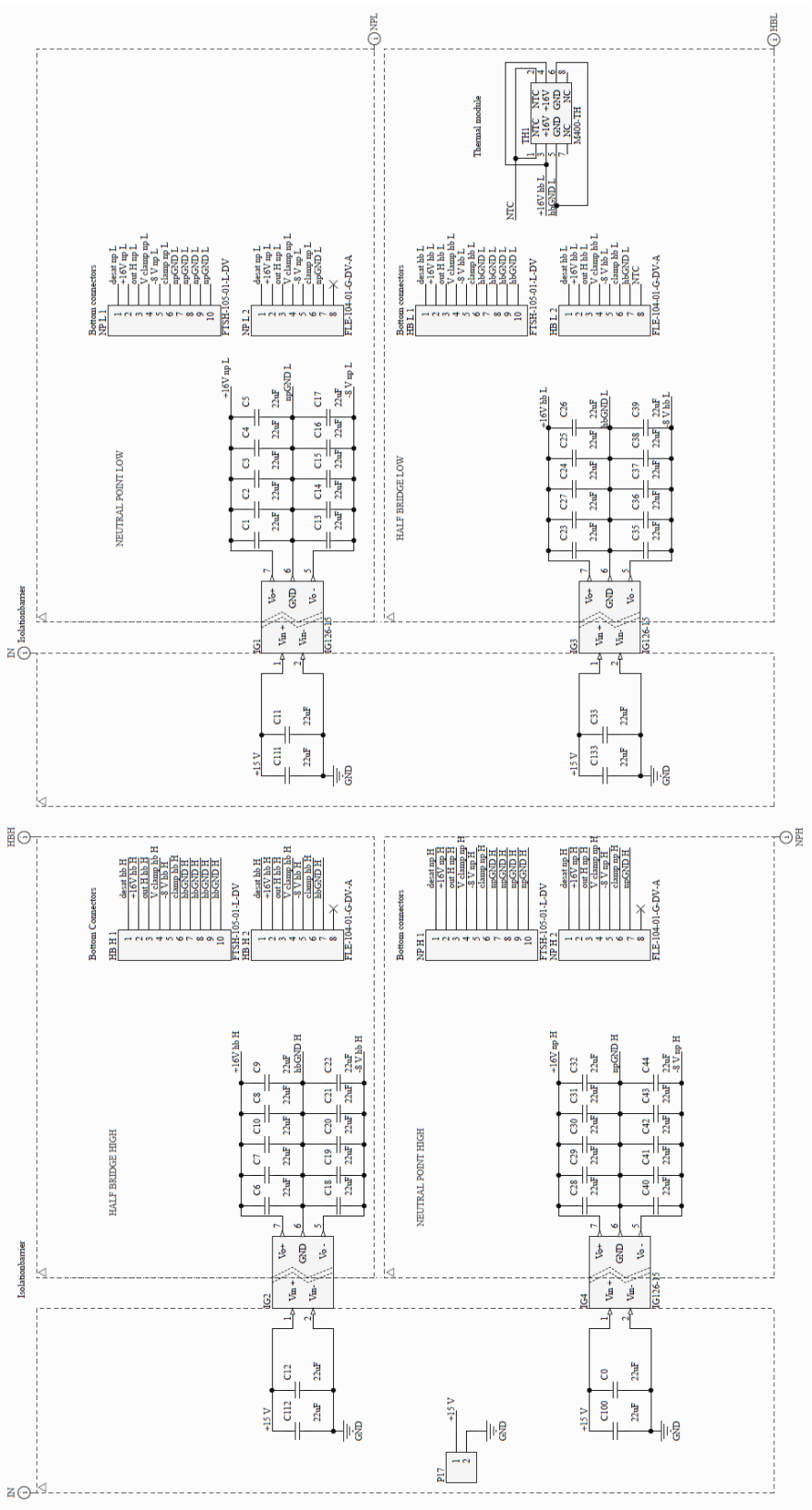

Figure 22: IN-PCB-SLAVE

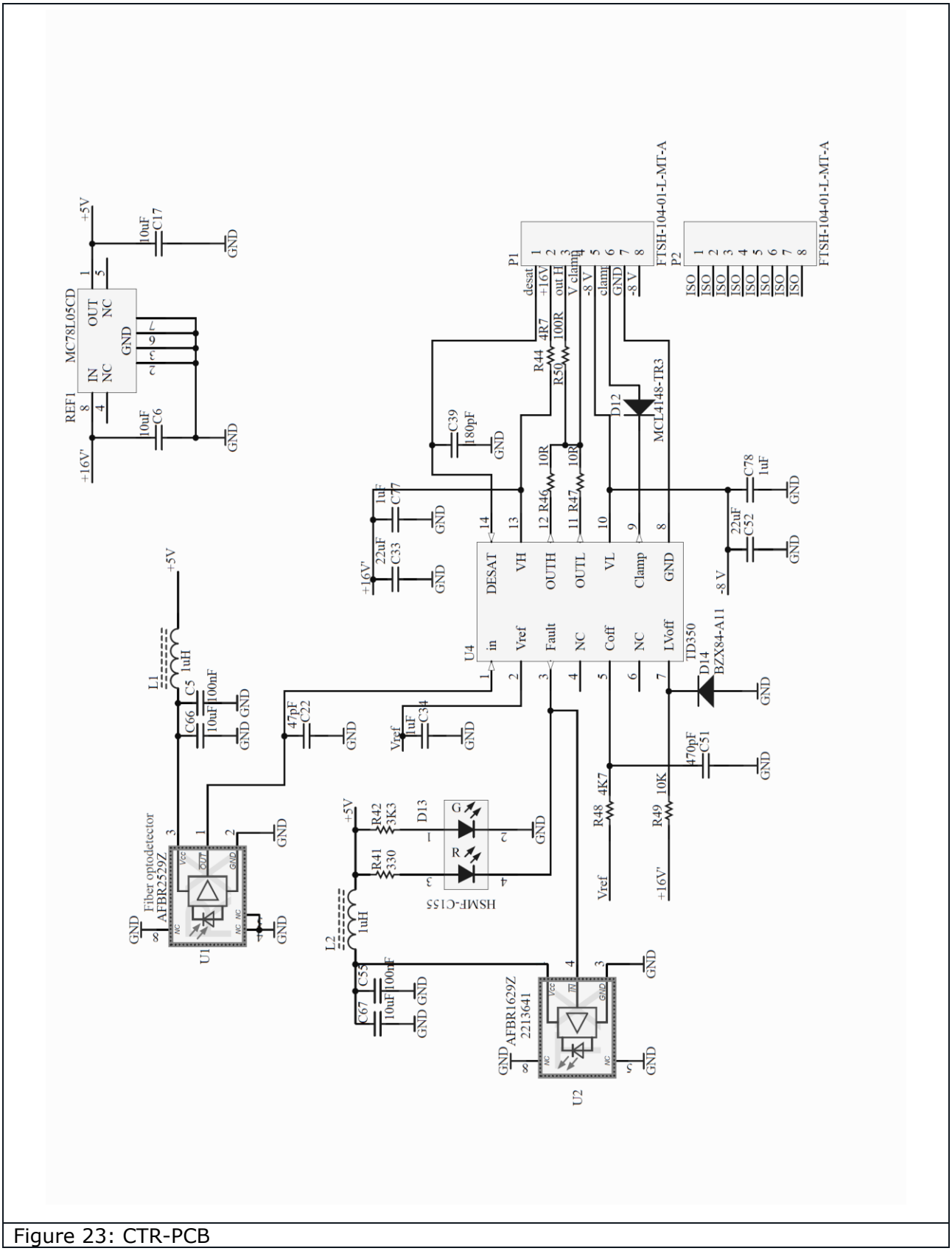

Figure 23: CTR-PCB

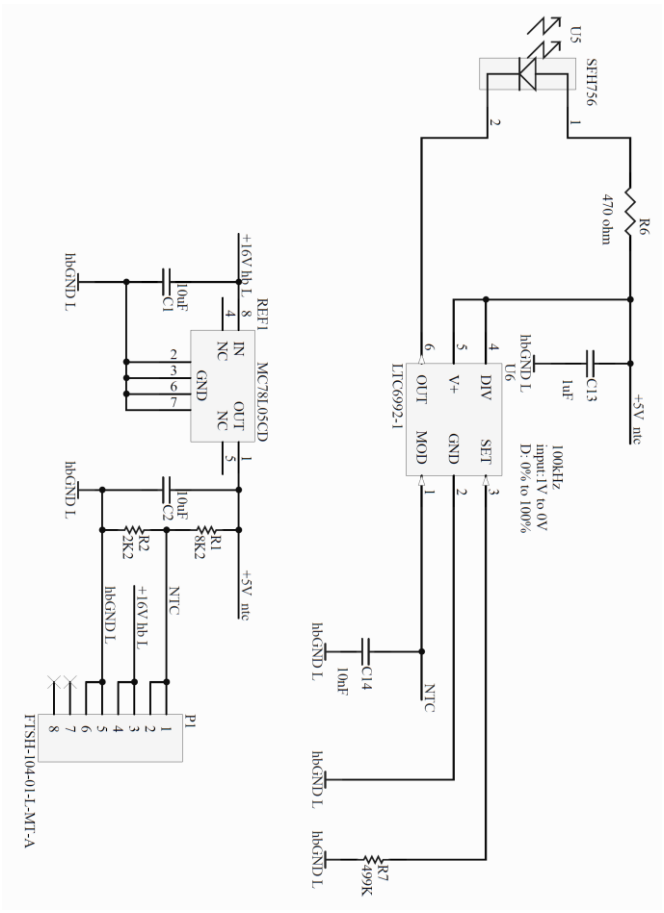

Figure 24: TH-PCB

8 Ordering numbers

Vincotech offer the LD00FP7X gate driver solution as a ready to use kit, including the input DC connector (+15V) screws and standoffs for assembling. Table 5 shows the ordering numbers for an S-M-S gate driver suitable for LD00FP7X.

Ordering number	BOM	Quantity	Obs.
GD-LD00-SMS-KIT	GD-LD00-Master	1	including input power connector, fiber optics connector, screws and standoffs
	GD-LD00-Slave	2	including input power connector, screws and standoffs
	GD-L400-SMS-CONN	4	

Table 5: Ordering numbers for an LD00 gate driver

9 BOM

9.1 BOM CTR-PCB

Description	Material group	Quantity	Un	Layout position
CGD-M400-PCB_CTR(REV06)	PCB	1	PC	PCB
C-1uF-25V-10%-X7R-0805-PM	Cap. below 500V	4	PC	C5; C34; C77; C78
C-10uF-25V-10%-X7R-1206-PM	Cap. below 500V	2	PC	C6; C17
C-47pF-100V-NPO-0805-PM; SAMPLE	Cap. below 500V	1	PC	C22
C-22uF-25V-10%-X7R-1210-PM	Cap. below 500V	2	PC	C33; C52
C-180pF-50V-5%-COG-0603-PM	Cap. below 500V	1	PC	C39
C-470pF-50V-5%-COG-0805-CM(I)	Cap. below 500V	1	PC	C51
LED-HSMF-C155-(Red/Green)-SMD-PM; SAMPLE	LEDs	1	PC	D13
DI-BZX84C10-SOT23	Diode zener	1	PC	D14
CONNECTOR-8PIN-1.27mm-MT-PM; SAMPLE	Connectors	2	PC	P1, P2
R-470R-1%-TK100-0805-CM(I)	Resistors	1	PC	R39
R-1K-1%-TK100-0805-CM(I)	Resistors	1	PC	R41
R-4K7-1%-0805-PM	Resistors	1	PC	R48
R-4R7-1%-TK100-0805-CM(I)	Resistors	1	PC	R44
R-10R-1%-TK100-0805;Sample	Resistors	2	PC	R46, R47
R-15K-1%-TK100-0805-PM; SAMPLE	Resistors	1	PC	R42
300758 R-10K-1%-TK100-0805-CM(I)	Resistors	1	PC	R49
R-100R-1%-TK100-0805; Sample	Resistors	1	PC	R50
MC78L05ACDR2G; Sample	IC	1	PC	REF1
SFH551/1-1V-PM; SAMPLE	IC	1	PC	U1
SFH756V-PM; SAMPLE	IC	1	PC	U2
IC-TD350ID-SO14-PM;Sample	IC	1	PC	U4

9.2 BOM TH-PCB

Description	Material group	Quantity	Un	Layout position
CGD-M400-PCB_TH(Rev03); SAMPLE	PCB	1	PC	PCB
C-10uF-25V-10%-X7R-1206-PM	Cap. below 500V	2	PC	C1, C2
C-1uF-25V-10%-X7R-0805-PM	Cap. below 500V	1	PC	C13
C-10nF-50V-10%-X7R-0805-CM(I)	Cap. below 500V	1	PC	C14
CONNECTOR-8PIN-1.27mm-MT-PM; SAMPLE	Connector	1	PC	P1
R-8K2-0.1%-TK25-0805-PM; SAMPLE	Resistors	1	PC	R1
R-2K2-0.1%-TK25-0805-PM; SAMPLE	Resistors	1	PC	R2
R-470R-1%-TK100-0805-CM(I)	Resistors	1	PC	R6
R-499K-1%-TK100-0805 PM; SAMPLE	Resistors	1	PC	R7
MC78L05ACDR2G; Sample	IC	1	PC	REF1
SFH756V-PM; SAMPLE	IC	1	PC	U5
IC-LTC6992CS6-1-SOT363-6L-PM; SAMPLE	IC	1	PC	U6

9.3 BOM IN-PCB MASTER (SLAVE)

Description	Material group	Quantity	Un	Layout position
CGD-LD00-PCB_IN(Rev01)	PCB	1	PC	
DRV-LD00-PCB_CTR(Rev51)	SemiFinished Good	4	PC	HBH CTR, NPH CTR, NPL CTR, HBL CTR-MASTER NA-SLAVE
C-47pF-100V-NPO-0805-PM	Capacitor	2	PC	C45,C46-MASTER NA-SLAVE
C-22uF-25V-10%-X7R-1210-PM	Capacitor	48	PC	C0-C33,C35-C44,C100,C111,C112,C133

CONNECTOR-10PIN-1.27mm-FTSH10-PM	Connector	4	PC	HB_H_1,HB_L_1,NP_H_1,NP_L_1
CONNECTOR-8PIN-1.27mm-FLE8-PM	Connector	4	PC	HB_H_2,HB_L_2,NP_H_2,NP_L_2
IC-IGC136-15W_DC/DC_CONVERTER	IC	4	PC	IG126_15-IG126_18
CONNECTOR-2PIN-2.5mm-HDR1X2-PM	Connector	1	PC	P17

9.4 BOM OUT-PCB

Description	Material group	Quantity	Un	Layout position
CGD-LD00-PCB_OUT(Rev01)	PCB	1	PC	PCB
C-22uF-25V-10%-X7R-1210-PM	Capacitor	24	PC	C1-C8,C13-C24,C29-C32
C-1uF-25V-10%-X7R-0805-PM	Capacitor	4	PC	C25,C34,C36,C37
C-100nF-50V-10%-X7R-0805-CM(I)	Capacitor	4	PC	C33,C35,C38,C39
DI-EGF1T-E3/67A-DO214BA-PM; SAMPLE	Diode	4	PC	D1,D2,D9,D10
DI-P6SMB18CA-18V-600W-SMB; Sample	Diode	8	PC	D3-D6,D11-D14
DI-VS-10BQ100PBF-SMB-PM; SAMPLE	Diode	4	PC	D7,D8,D15,D16
DI-P6SMB480A-480V-600W-5%-SMB; Sample	Diode	8	PC	D17,D18,D23,D24,D33-D36
BAS385 30V,200mA MICROMELF; Sample	Diode	12	PC	D19-D22,D25-D32
CONNECTOR-8PIN-1.27mm-SMD-FTSH8; SAMPLE	Connector	4	PC	HB_H,HB_L,NP_H,NP_L
TR-ZXTP25040DFH-PNP-SOT23; Sample	Transistor	4	PC	Q1-Q4

R-1K-1%-TK100-0805-CM(I)	Resistor	4	PC	R2,R23,R24,R47
R-8R2-1%-TK100-0603; Sample	Resistor	12	PC	R3,R4,R13-R16,R25,R26,R35-R38
R-R510-1%-TK100-1210-PM; SAMPLE	Resistor	12	PC	R7-R10,R29-R32
R-R25-5%-1210	Resistor	8	PC	R5-6;R21-22;R27-28;R43-44
R-15K-1%-TK100-0805-PM; SAMPLE	Resistor	8	PC	R17-R20,R39-R42
R-1R-1%-TK100-0805-CM	Resistor	4	PC	R45,R48,R51,R52
R-10R-1%-TK100-0805-PM; SAMPLE	Resistor	4	PC	R1,R46,R49,R50
TR-ZXGD3006E6-SOT23-6-PM; SAMPLE	IC	8	PC	T1-T8

10 Conclusion

With a proper parallel connection of the current boosters the current capability of the gate driver can be increased in order to serve the higher current rated Vincotech power modules, meanwhile the equal current sharing between the paralleled power modules is kept. To maintain this balanced current the customer has to pay a special attention to a symmetrical connection of the input-output wiring.