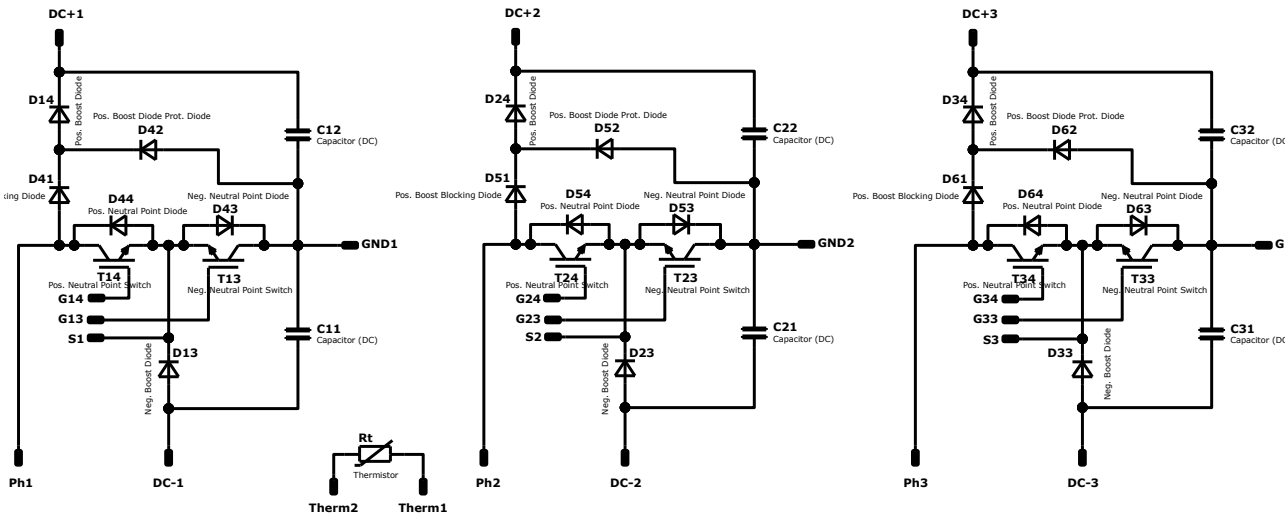
Vincotech

ANPFC-Advanced Neutral Boost PFC

General operation of ANPFC



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Revision History

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05.05.2023	1.0	Initial release	31
11.02.2023	2.0	ANPFC with MOSFET	24,25

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1 Abstract

Power demand from the grid continues to rise from year to year, making the development of efficient three-phase power factor correction topologies increasingly important. Several well-established PFC solutions have been published over the past years. This application note presents the ANPFC, a new, revolutionary PFC topology. Like three-phase PFC, the ANPFC targets EV chargers, industrial drives, UPS, and three-phase power supply markets. This application note highlights how the ANPC (ANPFC-Advanced Neutral Boost PFC) and the three-level PFC topologies it builds on stand out against other topologies. It offers a detailed explanation of the topology and its functionality. Moreover, it compares the topology with the other well-known three-phase PFCs in terms of performance and operation, as well as loss distribution and component power loss calculations.

2 Introduction

Power factor correction (PFC) aims to improve the power factor and, therefore, the power quality of power electronics applications. The power factor describes the ratio between the power actively used by electrical equipment to generate useful output – known as real power – and power that is consumed but not used directly – known as reactive power. While a load connected to an AC circuit with non-zero reactance generates a current that is out of phase with the voltage, a PFC circuit generates a current that is in phase with the phase voltage (current in phase).

This application note presents the advantages of the ANPFC topology against other well-known PFC topologies as well as the ANPFC's general operation and its system benefits. It further compares a virtual 650 V/30 A-rated ANPFC/NPFC/SPFC and a Vienna rectifier in terms of their efficiency.

3 Topology description

Figure 1 illustrates the basic cell of the ANPFC topology.

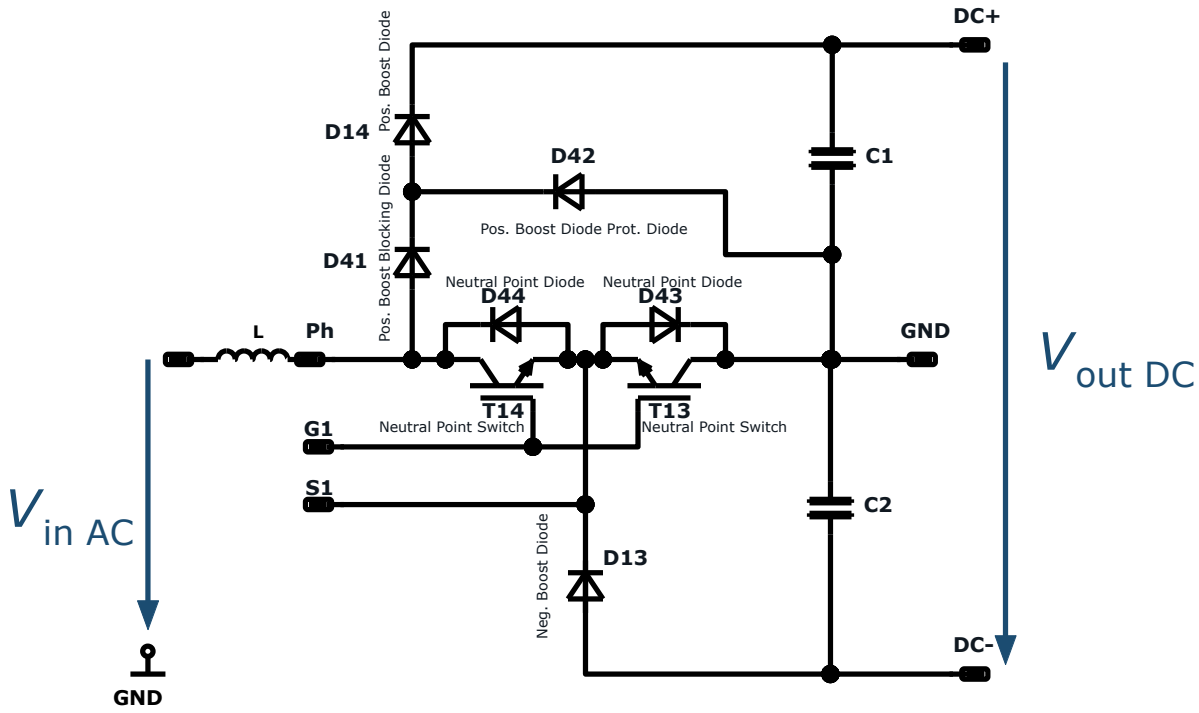


Figure 1: One phase ANPFC

Short description of the components:

- Neutral point IGBTs (T13&T14): These are the topology's main switches, with T14 being a positive boost switch and T13 a negative boost switch.
- Neutral point diodes (D43&D44): Neutral blocking diodes and rectifier diodes select the positive or negative current paths for the main switches. D43 in paired with T14 create a reverse blocking IGBT, as do D44 and T13.
- Boost diodes (D14&D13): Fast positive and negative boost diodes. D13 in combination with T13 form the negative commutation pair, while D14 and T14 form the positive commutation pair.

- D41 rectifier diode: This diode is used mainly to increase the voltage blocking capability of D14.
- D42 fast protection diode: This diode clamps the two serial connected diodes middle point to GND.

Structure:

The positive side rectifier ***neutral point diode*** **(D43)** selects the positive side of the input voltage and, thereby, the positive current direction. During the positive current (the positive half of the sine wave) the **neutral point switch (T14)** energises the input choke (L) by connecting the input (Ph) to GND. Switching off T14 causes the energized input choke to freewheel through the **positive boost blocking diode (D41)** and the **positive boost diode (D14)** to DC+. The ***neutral point diode*** **(D44)** selects the negative sine wave**.** During the negative half of the sine wave, the choke is energized by turning on **T13**. In this state, the choke connects the instantaneous negative input voltage and GND. D13 enables negative boost freewheeling through D44.

Application:

A typical application of three-level ANPFC topologies is the three-phase system. The ANPFC can also be used in single phase system but with the drawback of requiring a large DC link capacitor bank. The DC+➔ NEURTAL, and DC-➔ NEUTRAL capacitors must each supply the output current during one half sine wave. When the active side is operating, the current from the inactive side must be supplied by the DC link capacitor. Only the positive or negative DC link capacitor is charged during each half sine wave of the input phase.

How it works:

The input rectifier selects the positive or negative input voltage for the positive or negative side-boost PFC circuit. The input choke with the positive side-boost PFC circuit generates the DC+ referenced to NEUTRAL, while the input choke with the negative side-boost PFC generates the DC- referenced to NEUTRAL.

By introducing the middle potential (NEUTRAL), the components in the ANPFC are only exposed to half the output voltage.

Reducing the switched voltage to half the output voltage offers three-level PFC topologies the following advantages:

- The voltage rating of all required components is halved compared to the two-level topology with same output voltage, reducing static and dynamic losses for active components and cutting component costs.

- The inductor current ripple at the same switching frequency and inductance are also halved because the switched voltage is 50% lower than in the corresponding two-level topology.

$$\Delta I = \frac{\Delta t * \Delta U}{L}$$

Keeping the same switching frequency, the same current ripple can be achieved using an inductor with half the inductance. Alternatively, with the same magnetic device, the switching frequency can be reduced by half compared to the two-level topology while exposing the choke to the same current ripple.

- A single rectifier diode can be used for the positive and negative input current paths. Meanwhile, the two-level boost PFC's input current passes through two rectifier diodes.

Identification table:

Reference designator	Function/ Function name in topology	Voltage stress	Typical breakdown voltage *depends on system voltage	Typical component technology
T13, T14	Boost switch Neutral point switch	$V_{out\ DC}/2$	650, 950 V	High speed IGBT, WBG
D13, D14	Boost diode Positive / negative boost diode	$V_{out\ DC}/2$	650, 950 V	Fast recovery diode, SiC Schottky diode
D43, D44	Rectifier diode Neutral point diode	$V_{out\ DC}/2$	1600 V	50/60 Hz rectifier diode
D41	Positive boost blocking diode	Vdc/2	1600 V	50/60 Hz rectifier diode
D42	Positive boost diode Protection diode	Vdc/2	650, 950 V	Fast recovery diode

3.1 From the NPFC to the ANPFC topology

The NPFC (also referred to as the Vienna rectifier) is a derivation of the MNPC (T-type NPC) topology in which the buck switches (half bridge switches) are removed and the inverter is operated in boost mode (cos φ =-1), as shown in Figure 2 (a).

Here, we detail the modifications required to go from the NPFC to the ANPFC topology step by step and highlight the ANPFC topology's advantages.

While a two-level boost PFC boosts the 220 V_{AC} input phase voltage to 400 V DC link, the total DC link voltage achieved using a three-level boost topology is 800 V. Because in the NPFC topology, the **DC boost** diodes have to block the full DC link voltage, as shown in Figure 2 (a), the voltage rating of the boost diodes must be 1200 V.

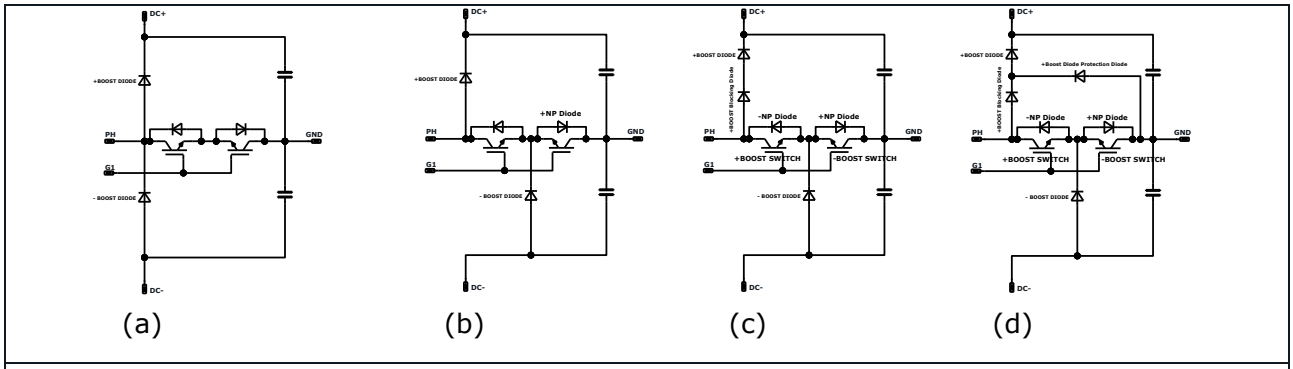


Figure 2: From the NPFC to the ANPFC topology

- **Modification #1**: Reducing the topology's losses
  - The –***boost diode*** (*negative boost diode*) is moved to the common emitter point of the boost switches, as shown in figure 2 (b).

  With this modification of the topology, the voltage rating of the –***boost diode*** can be reduced from 1200 V to 600 V. This modification is enabled by +***NP diode,*** which clamps the cathode of the ***–boost diode*** to GND. In the NPFC topology, the cathode of the –***boost diode*** can reach the potential at DC+; meanwhile, in the ANPFC topology, the ***–boost diode's*** cathode cannot exceed GND potential. This makes it possible to replace the 1200 V rated diode with one rated at 600-650 V. This modification reduces the static and switching losses of the ***–boost diode.*** Replacing the 1200 V diode with a 600 V diode further reduces the turn-on losses of the ***–boost switch***. Before the modification of the NPFC, an IGBT rated at 650 V commutated with a 1200 V diode. Following the modification, the commutation pair was made up of a 650 V IGBT and a 650 V FWD, reducing the E_{on} of the IGBT as well as the ***–boost diode's*** static and dynamic losses.

- **Modification #2**: Additional topology loss reduction:
  - A ***+boost blocking diode*** is added in series connected with the ***+boost diode***, as shown in figure 2 (c), allowing to reduce the +***boost diode's*** (*positive boost diode*) voltage rating from 1200 V to 600 V.

  The positive boost diode's voltage rating cannot be reduced by positioning it elsewhere in the topology. That's why a series ***+boost blocking diodes*** is introduced in the circuitry. Adding a series diode to the positive boost diode makes it possible to reduce its voltage rating to 600 V, bringing the advantages of a 600 V commutating diode with a 650 V rated IGBT, as on the negative side. Because two diodes connected in series generate higher static losses, a rectifier type diode is used as the ***+boost blocking diode***.
- **Modification #3**:
  - A ***+boost diode protection diode*** is added, as shown in figure 2 (d).

  The +***boost blocking diode*** was added to the circuit to reduce the static and dynamic losses of the positive commutation loop (+boost switch, +boost diode). A rectifier type diode was selected for the ***+boost blocking diode*** to minimize the static loss increase during freewheeling of the input current. If two diodes are serially connected, the fast diode (+***boost diode***) always commutates first as its reverse recovery time is shorter. The fast diode blocks the voltage while the slow (***+boost blocking diode)*** remains in reverse recovery. As long as the ***+boost blocking diode*** is in reverse recovery, its blocking capability is zero, and the phase potential is supplied to the anode of the +***boost diode***. When the input voltage crosses zero, the positive side of the topology stops operating and the negative side kicks in. At that moment, the +***boost blocking diode*** is still in reverse recovery and the phase potential and, implicitly, the common point potential of the serial connected diodes receive the DC- potential. That means that the +***boost diode*** could be exposed to the full DC link voltage (800 V). To avoid overvoltage of the +***boost diode*** during zero crossing of the input voltage, the middle point (anode of +***boost diode***) is clamped to GND by adding the ***+boost diode protection diode*** to the circuit. During reverse recovery of the ***+boost blocking diode***, the reverse recovery current is supplied by the ***+boost diode protection diode.*** As pointed out earlier, this diode serves a protective function and does not handle any current. As a result, its power loss can be considered zero and need not be included in the total power loss of the topology.

3.2 Calculation of the modulation index and duty cycle for the three-level ANPFC

This chapter presents the continuous conduction mode (CCM) boost PFC calculation. To make the average input current follow the instantaneous line voltage, a fixed switching frequency is used. The switch duty cycle is a function of the instantaneous line voltage (pulse width modulation).

Based on the steady state assumption, in CCM:

$$t_{ON}(\mathrm{t}) * |V_{in\ AC}(t)| = [T - t_{ON}(\mathrm{t})] * \left[\frac{V_{out\ DC}}{2} - |V_{in\ AC}(t)|\right]$$

The switch duty cycle is introduced as:

$$D(t) = \frac{t_{ON}(\mathrm{t})}{T}$$

This makes the duty cycle:

$$D(t) = 1 - \frac{|V_{in\ AC}(t)|}{\frac{V_{out\ DC}}{2}}$$

The modulation index is introduced as:

$$M_i = \frac{V_{in\ AC\ pk}}{\frac{V_{out\ DC}}{2}}$$

If the input voltage equals:

$$V_{in\ AC}(t) = V_{in\ AC\ pk} * \sin(\omega t),$$

the ANPFC **switch** duty cycle in CCM mode is:

$$D(t) = 1 - M_i * |\sin(\omega t)|,$$

and the ANPFC **FWD** duty cycle in CCM mode is:

$$D(t) = M_i * |\sin(\omega t)|.$$

In conclusion, the ANPFC duty cycle and modulation index can be calculated with the two-level boost PFC formulas by replacing the two-level output voltage with the half DC link voltage of the three-level topology. The ANPFC topology should use the same PWM pattern as the NPFC topology and other three-level PFC topologies.

3.3 Modulation and control scheme for ANPFC considering the single-phase topology

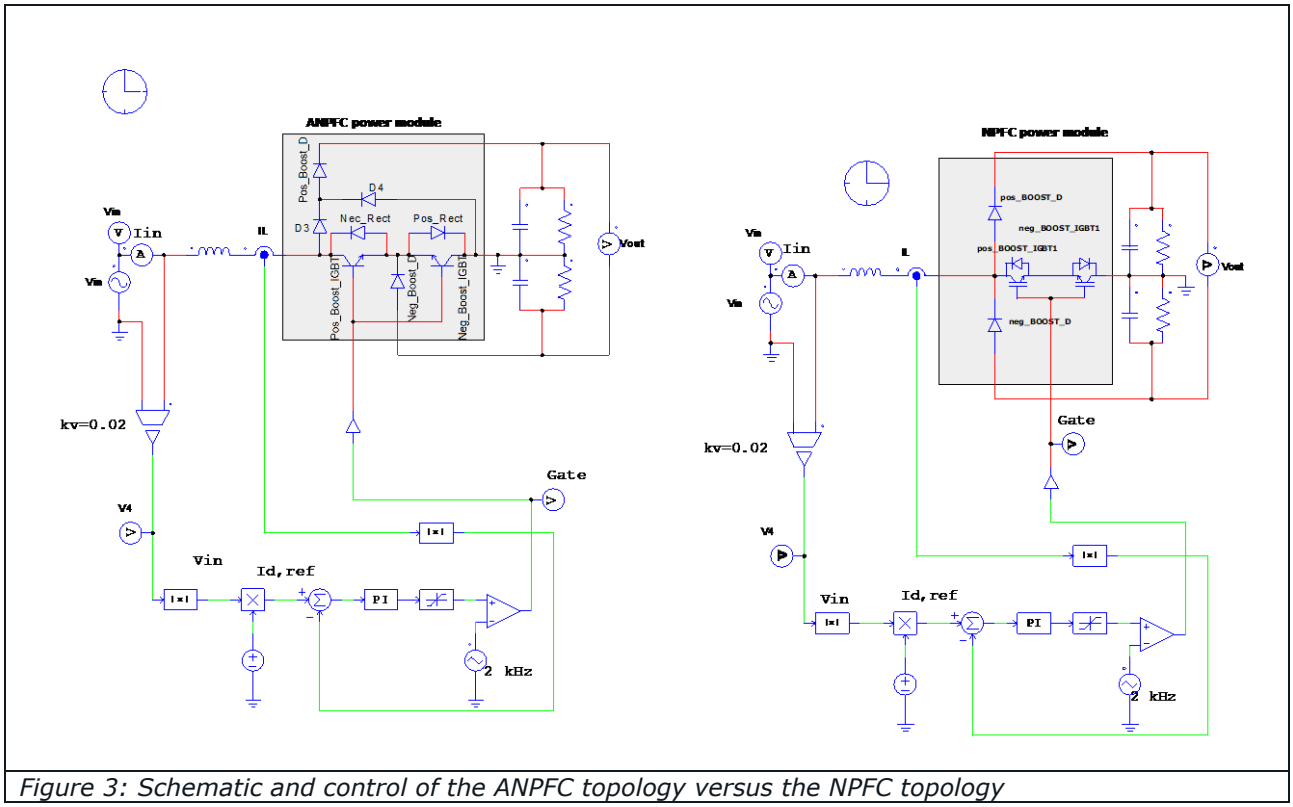
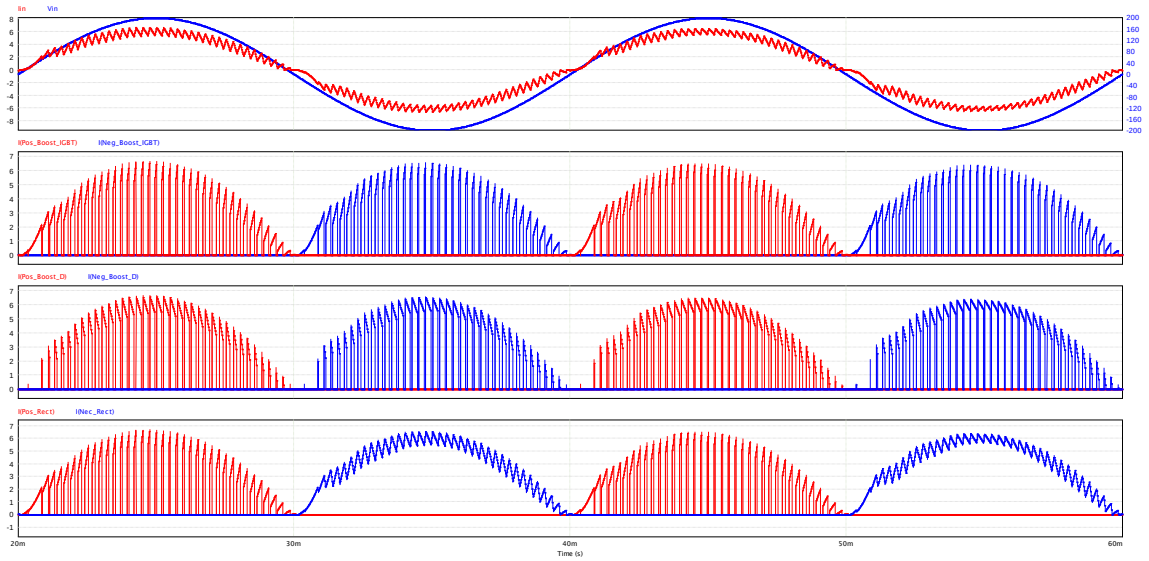


Figure 3: Schematic and control of the ANPFC topology versus the NPFC topology

Comparing the control logic of the ANPFC shown in **Figure 3** with the control logic of the two-level boost PFC reveals that both are identical up to the inductor current measurement. Because the choke current is bidirectional, the current sensor output signal must be rectified. The NPFC, SPFC, or Vienna rectifier control logic can be used to control the ANPFC topology without any modification, as shown in Figure 3.

ANPFC waveforms



NPFC waveforms

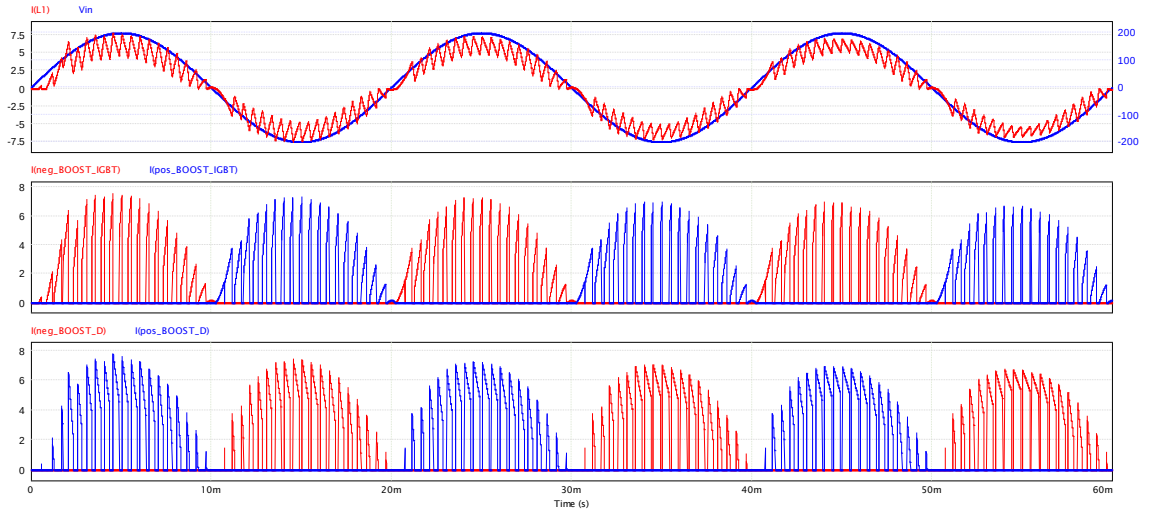


Figure 4: Input voltage, input current, and typical device current waveforms of the ANPFC and NPFC

3.4 Modulation and control scheme for ANPFC considering the three-phase topology

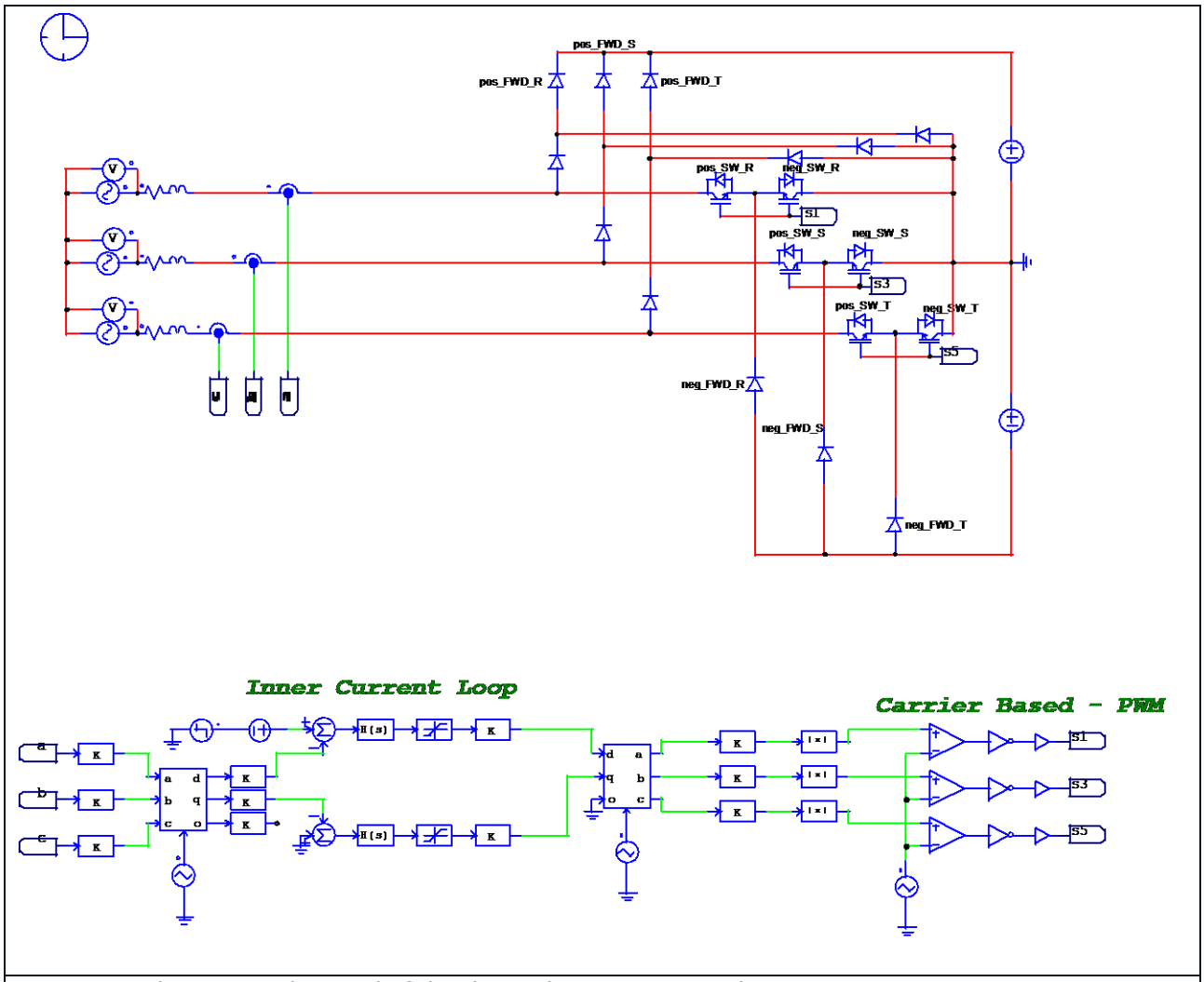


Figure 5: Schematic and control of the three-phase ANPFC topology

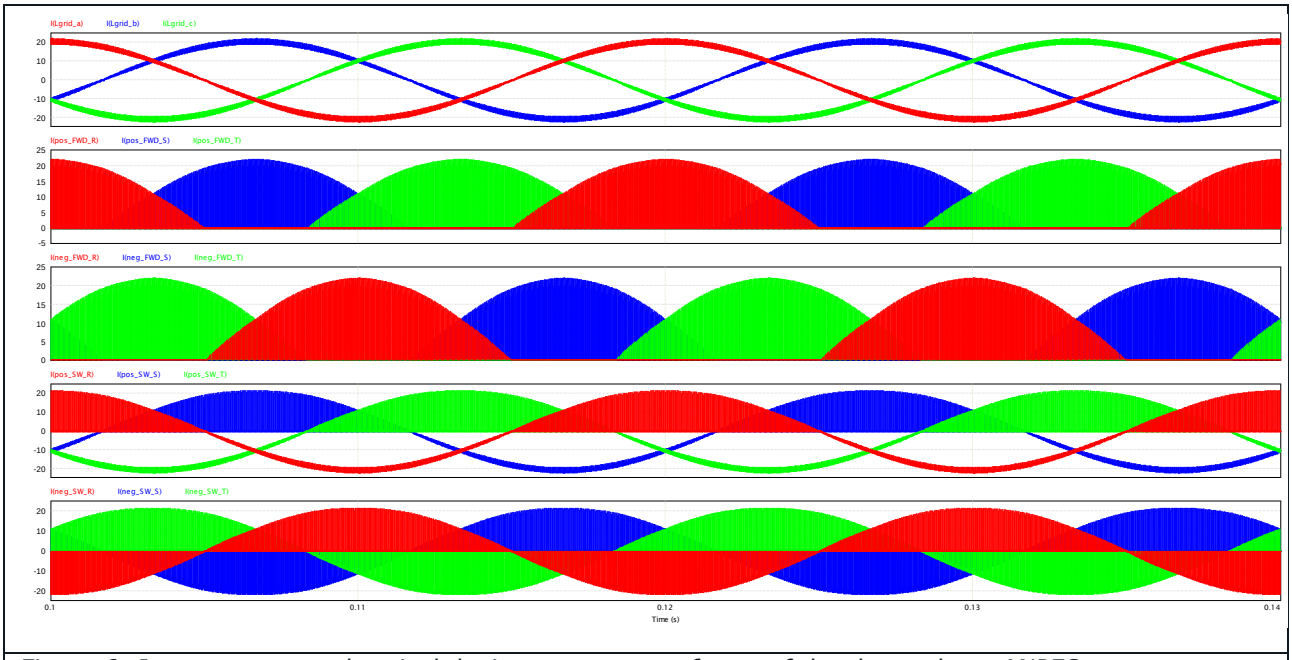
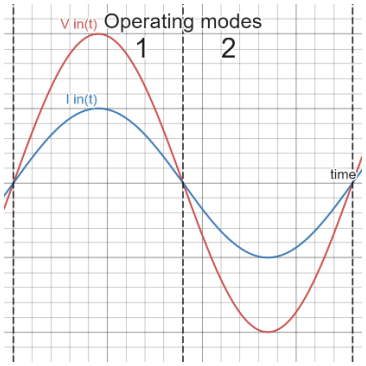


Figure 6: Input current and typical device current waveforms of the three-phase ANPFC

Note that the negative current over the positive boost switches means that the reverse diode conducts continuously. Meanwhile, the reverse diodes of the negative boost switches conduct only the positive boost switch's current, which is a switched current.

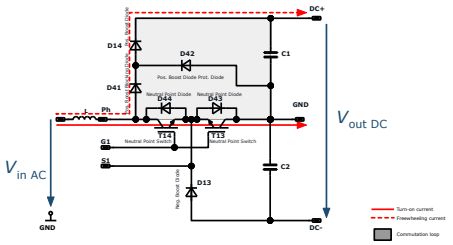
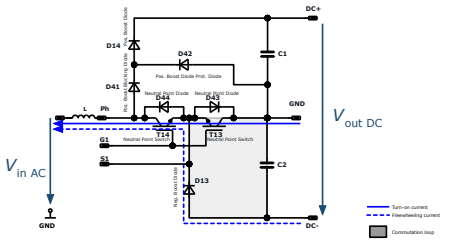
3.5 Commutation loops and current paths in the three-level ANPFC

The following operating modes can be identified as a function of the input voltage:



- Operating mode 1: $V_{in\ AC} > 0$
- Operating mode 2: $V_{in\ AC} < 0$

3.5.1 Current paths, commutation loops, and loss distribution of the topology

	1		2	
	$V_{in\ AC}>0$		$V_{in\ AC}<0$	
				
Operation mode/ function	1		2	
	Static	Dynamic	Static	Dynamic
Positive boost diode (D14)	(D)	YES	N.O.	N.O.
Neutral point switch (T14)	(1-D)	YES	N.O.	N.O.
Positive boost blocking diode (D41)	(D)		N.O.	N.O.
Neutral point diode (D43)	(1-D)		N.O.	N.O.
Negative boost diode (D13)	N.O.	N.O.	(D)	YES
Neutral point switch (T13)	N.O.	N.O.	(1-D)	YES
Neutral point diode (D44)	N.O.	N.O.	(1)	

Here:

(1) is the static loss of a component conducting with duty cycle 1.

(D) is the static loss of a component conducting with duty cycle D.

(1-D) is the static loss of a component conducting with duty cycle 1-D.

N.O. Not operating.

Note that the positive rectifier diode (D43) conducts only when positive boost IGBT (T14) is conducting. Meanwhile, the negative rectifier diode (D44) conducts during the entire negative period of the input current.

The total rectifier loss during the positive period of the input sine wave is equal to the rectifier loss during the negative period: During the positive energizing period, rectifier conduction losses are at D43 with a duty cycle 1-D. During freewheeling, the rectifier losses are at D41 with duty cycle D. Adding the rectifier's static losses leads to a full sine wave rectifier loss like

on negative side of the module. Furthermore, distributing the rectifier losses that occur under positive input voltage to two diodes positively impacts the rectifier's junction temperatures.

4 Average static and dynamic semiconductor power losses calculation of the ANPFC

The average static losses of a device in conduction can be calculated as the integral of the product of device's current and its voltage drop over one fundamental period of the input/output voltage.

$$P_{st} = \frac{1}{T} * \int_0^{T/2} U_{IGBT}(I_{IGBT}(t)) * I_{IGBT}(t) * d(t) \qquad \textbf{(1)}$$

Here, the average static losses are calculated using a linear model. The device voltage drop is considered as:

$$V_{CE} = v_{t0} + I_C * r_t$$

with

$$v_{t0} - threshold\ voltage$$

$$r_t - dynamic\ resistance$$

Because the threshold voltage and dynamic resistance used to calculate the average losses are temperature dependent parameters, they must be considered at an anticipated junction temperature. Once the power loss calculation has been performed at the anticipated junction temperature, the real average junction temperature can be recalculated. Repeating this procedure several times allows to determine the exact average power and junction temperature.

In three-level inverters with a duty cycle that can be expressed as:

$$D(t) = \frac{|V_{out\,AC}(t)|}{\frac{V_{in\,DC}}{2}},$$

the primitive function of integral **(1)** for the components with duty cycle D is:

$$P_{st(D)} = r_t * I^2_{ph(RMS)} * \frac{M_i}{12\pi} * \int [\cos(3\omega t + \varphi) - 3\cos(\omega t - \varphi) - 6\cos(\omega t - \varphi)]\, dt + v_{t0} * \sqrt{2} * I_{ph(RMS)} * M_i * \int \left[\frac{\cos(\varphi)}{2T} \mathrm{t} - \frac{\sin(2\omega t + \varphi)}{8\pi}\right] dt. \qquad \textbf{(2)}$$

Comparing the general formula used to calculate static losses with expression **(2),** the primitive functions of the RMS and AVG current of the device with duty cycle D can be determined:

$$P_{st(D)} = r_t * I^2_{(RMS)(D)} + v_{t0} * I_{(AVG)(D)}$$

$$I^2_{(RMS)(D)} = I^2_{ph(RMS)} * \frac{M_i}{12\pi} * \int [\cos(3\omega t + \varphi) - 3\cos(\omega t - \varphi) - 6\cos(\omega t - \varphi)]\, dt$$

$$I_{(AVG)(D)} = \sqrt{2} * I_{ph(RMS)} * M_i * \int \left[\frac{\cos(\varphi)}{2T}\mathrm{t} - \frac{\sin(2\omega t+\varphi)}{8\pi}\right] dt$$

Similarly, the primitive function of integral **(1)** for the components with duty cycle 1-D is:

$$P_{st(1-D)} = r_t * I^2_{ph(RMS)} * \int \left[\frac{t}{T} - \frac{1}{4\pi}\sin(2\omega t) - \frac{M_i}{12\pi}[\cos(3\omega t + \varphi) - 3\cos(\omega t - \varphi) - 6\cos(\omega t + \varphi)]\right] dt + v_{t0} * \sqrt{2} *$$

$$I_{ph(RMS)} \int \left[-\frac{\cos(\omega t)}{2\pi} - M_i\left[\frac{\cos(\varphi)}{2T}t - \frac{\sin(2\omega t+\varphi)}{8\pi}\right]\right] dt$$

The primitive functions of the RMS and AVG current of the device with duty cycle 1-D are:

$$I^2_{(RMS)(1-D)} = I^2_{ph(RMS)} \int \left[\frac{t}{T} - \frac{1}{4\pi}\sin(2\omega t) - \frac{M_i}{12\pi}[\cos(3\omega t + \varphi) - 3\cos(\omega t - \varphi) - 6\cos(\omega t + \varphi)]\right] dt$$

$$I_{(AVG)(1-D)} = \sqrt{2} * I_{ph(RMS)} \int \left[-\frac{\cos(\omega t)}{2\pi} - M_i\left[\frac{\cos(\varphi)}{2T}t - \frac{\sin(2\omega t+\varphi)}{8\pi}\right]\right] dt$$

The general case of the voltage-current relationship with a phase shift ø is represented in Figure 7:

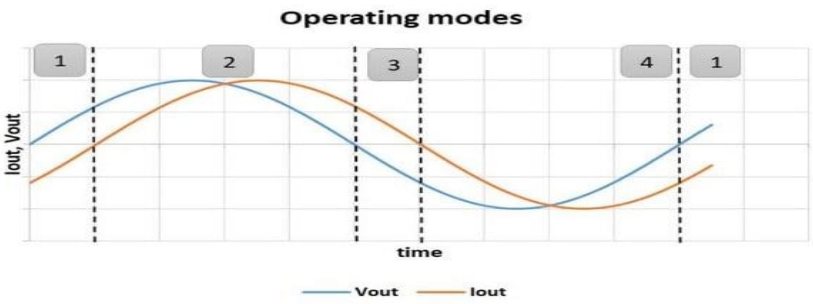


Figure 7: Output voltage, output current of an inverter

Considering the output current as a reference and integrating the primitive function of D and 1-D between the limits [0 ➔ (Π-Φ)] in operating mode 2 (real mode) and [(Π-Φ) ➔ Π] in operating mode 3 (reactive mode) and taking advantage of the topology's symmetry yields defined integrals that describe the loss of all components during one period of the output current.

Static losses in operating mode 2 **- [0 ➔ (Π-Φ)] (**real mode):

Components with duty cycle D:

$$I^2_{(RMS)(D)} = I^2_{ph(RMS)} * \frac{4}{3} * \frac{M_i}{\pi} * cos^4\left(\frac{\varphi}{2}\right) \qquad \textbf{(3)}$$

$$I_{(AVG)(D)} = \frac{\sqrt{2}*I_{ph(RMS)}*M_i}{4\pi}[(\pi-\varphi)\cos(\varphi)+\sin(\varphi)] \quad \textbf{(4)}$$

Components with duty cycle 1-D:

$$I^2_{(RMS)(1-D)} = I^2_{ph(RMS)}\left[\frac{\pi-\varphi}{2\pi}+\frac{\sin(2\varphi)}{4\pi}-\frac{4}{3}*\frac{M_i}{\pi}*cos^4\left(\frac{\varphi}{2}\right)\right] \quad \textbf{(5)}$$

$$I_{(AVG)(1-D)} = \frac{\sqrt{2}*I_{ph(RMS)}}{2\pi}\left[\cos(\varphi)+1-\frac{M_i}{2}[(\pi-\varphi)\cos(\varphi)+\sin(\varphi)]\right] \quad \textbf{(6)}$$

Components with duty cycle: 1 (continuous conduction)

$$I^2_{(RMS)(1)} = I^2_{(RMS)(D)}+I^2_{(RMS)(1-D)} = I^2_{ph(RMS)}\left[\frac{\pi-\varphi}{2\pi}+\frac{\sin(2\varphi)}{4\pi}\right] \quad \textbf{(7)}$$

$$I_{(AVG)(1)} = I_{(AVG)(D)}+I_{(AVG)(1-D)} = \frac{\sqrt{2}*I_{ph(RMS)}}{2\pi}[\cos(\varphi)+1] \quad \textbf{(8)}$$

Static losses in operation mode 3 **- [(П-Φ) → П]** (reactive mode):

Components with D:

$$I^2_{(RMS)(D)} = I^2_{ph(RMS)}*\frac{4}{3}*\frac{M_i}{\pi}*sin^4\left(\frac{\varphi}{2}\right) \quad \textbf{(9)}$$

$$I_{(AVG)(D)} = \frac{\sqrt{2}*I_{ph(RMS)}*M_i}{4\pi}[\sin|\varphi|-|\varphi|\cos(\varphi)] \quad \textbf{(10)}$$

Components with duty cycle 1-D:

$$I^2_{(RMS)(1-D)} = I^2_{ph(RMS)}\left[\frac{|\varphi|}{2\pi}-\frac{\sin(2\varphi)}{4\pi}-\frac{4}{3}*\frac{M_i}{\pi}*sin^4\left(\frac{\varphi}{2}\right)\right] \quad \textbf{(11)}$$

$$I_{(AVG)(1-D)} = \frac{\sqrt{2}*I_{ph(RMS)}}{2\pi}\left[1-\cos(\varphi)-\frac{M_i}{2}[\sin|\varphi|-|\varphi|\cos(\varphi)]\right] \quad \textbf{(12)}$$

Components with duty cycle: 1 (continuous conduction)

$$I^2_{(RMS)(1)} = I^2_{(RMS)(D)}+I^2_{(RMS)(1-D)} = I^2_{ph(RMS)}\left[\frac{|\varphi|}{2\pi}-\frac{\sin(2\varphi)}{4\pi}\right] \quad \textbf{(13)}$$

$$I_{(AVG)(1)} = I_{(AVG)(D)}+I_{(AVG)(1-D)} = \frac{\sqrt{2}*I_{ph(RMS)}}{2\pi}[1-\cos(\varphi)] \quad \textbf{(14)}$$

4.1 Static losses of boost switches (T13, T14)

As the three-level PFC is a special case of the three-level inverter with a phase shift Φ=Π, the boost switch average static losses can be calculated with the formulas (11) and (12) considering that the duty cycle of the switch is (1-D) as stated in loss distribution matrix.

$$I^2_{(RMS)(1-D)} = I^2_{ph(RMS)}\left[\frac{|\varphi|}{2\pi} - \frac{\sin(2\varphi)}{4\pi} - \frac{4}{3} * \frac{M_i}{\pi} * sin^4\left(\frac{\varphi}{2}\right)\right] \quad \textbf{(11)}$$

$$I_{(AVG)(1-D)} = \frac{\sqrt{2}*I_{ph(RMS)}}{2\pi}\left[1 - \cos(\varphi) - \frac{M_i}{2}[\sin|\varphi| - |\varphi|\cos(\varphi)]\right] \quad \textbf{(12)}$$

Boost switch static losses:

$$I^2_{(RMS)(1-D)} = I^2_{ph(RMS)}\left[\frac{1}{2} - \frac{4}{3} * \frac{M_i}{\pi}\right] \quad \textbf{(15)}$$

$$I_{(AVG)(1-D)} = \frac{\sqrt{2}*I_{ph(RMS)}}{2\pi}[2 + \pi] \quad \textbf{(16)}$$

$$P_{st-SW} = r_t * I^2_{(RMS)(1-D)} + v_{t0} * I_{(AVG)(1-D)}$$

4.2 Static losses of boost diodes (D13, D14)

Because the duty cycle of the boost diodes is D, their static losses can be calculated by substituting Φ with Π in formulas (9) and (10):

$$I^2_{(RMS)(D)} = I^2_{ph(RMS)} * \frac{4}{3} * \frac{M_i}{\pi} * sin^4\left(\frac{\varphi}{2}\right) \quad \textbf{(9)}$$

$$I_{(AVG)(D)} = \frac{\sqrt{2}*I_{ph(RMS)}*M_i}{4\pi}[\sin|\varphi| - |\varphi|\cos(\varphi)] \quad \textbf{(10)}$$

Boost diode static losses:

$$I^2_{(RMS)(D)} = I^2_{ph(RMS)} * \frac{4}{3} * \frac{M_i}{\pi} \quad \textbf{(17)}$$

$$I_{(AVG)(D)} = \frac{\sqrt{2}*I_{ph(RMS)}*M_i}{4} \quad \textbf{(18)}$$

$$P_{st-FWD} = r_t * I^2_{(RMS)(D)} + v_{t0} * I_{(AVG)(D)}$$

4.3 Static loss of rectifier diodes (D41; D43; D44)

As pointed out in the loss table, the duty cycles of the rectifier diodes are:

- D41: D
- D43: 1-D
- D44: 1

4.3.1 D41 static losses

The average static losses of conducting components with a duty cycle D can be expressed using formulas (17) and (18):

$$I^2_{(RMS)(D)} = I^2_{ph(RMS)} * \frac{4}{3} * \frac{M_i}{\pi} \quad \textbf{(17)}$$

$$I_{(AVG)(D)} = \frac{\sqrt{2} * I_{ph(RMS)} * M_i}{4} \quad \textbf{(18)}$$

$$P_{st-RECT(D)} = r_t * I^2_{(RMS)(D)} + v_{t0} * I_{(AVG)(D)}$$

4.3.2 D43 static losses

Given that D43 has a duty cycle of 1-D, its static losses can be calculated with formulas (15) and (16):

$$I^2_{(RMS)(1-D)} = I^2_{ph(RMS)} \left[\frac{1}{2} - \frac{4}{3} * \frac{M_i}{\pi}\right] \quad \textbf{(15)}$$

$$I_{(AVG)(1-D)} = \frac{\sqrt{2} * I_{ph(RMS)}}{2\pi} [2 + \pi] \quad \textbf{(16)}$$

$$P_{st-RECT(1-D)} = r_t * I^2_{(RMS)(1-D)} + v_{t0} * I_{(AVG)(1-D)}$$

4.3.3 D44 static losses

The duty cycle of D44 is 1, which means that its static losses can be calculated by substituting the Φ with Π in formulas (13) and (14):

$$I^2_{(RMS)(1)} = I^2_{(RMS)(D)} + I^2_{(RMS)(1-D)} = I^2_{ph(RMS)} \left[\frac{|\varphi|}{2\pi} - \frac{\sin(2\varphi)}{4\pi}\right] \quad \textbf{(13)}$$

$$I_{(AVG)(1)} = I_{(AVG)(D)} + I_{(AVG)(1-D)} = \frac{\sqrt{2} * I_{ph(RMS)}}{2\pi} [1 - \cos(\varphi)] \quad \textbf{(14)}$$

$$I^2_{(RMS)(1)} = I^2_{ph(RMS)} * \frac{1}{2} \quad \textbf{(19)}$$

$$I_{(AVG)(1)} = \frac{\sqrt{2} * I_{ph(RMS)}}{\pi} \quad \textbf{(20)}$$

$$P_{st-RECT} = r_t * I^2_{(RMS)(1)} + v_{t0} * I_{(AVG)(1)}$$

4.4 Switching losses

4.4.1 Boost IGBT switching losses

The general formula for the switching losses over half of the input sine wave is:

$$P_{sw} = f_{SW} * \frac{1}{T} * \int_0^{T/2} \left[E_{offIGBT}(I_{IGBT}(t)) + E_{onIGBT}(I_{IGBT}(t))\right] * d(t) \quad \textbf{(21)}$$

Here:

f_{sw} is the switching frequency,

$E_{offIGBT}(I_{IGBT}(t))$ is the IGBT's single-pulse switch-off energy, and

$E_{onIGBT}(I_{IGBT}(t))$ is the IGBT's single-pulse switch-on energy.

Assuming a linear dependency of the switching energy losses with the switched current, the following normalisation to the nominal current can be made:

$$E_{onIGBT}(I_{IGBT}(t)) = E_{on0} + \frac{I_{IGBT}(t)}{I_N} * (E_{onN} - E_{on0})$$

$$E_{offIGBT}(I_{IGBT}(t)) = E_{off0} + \frac{I_{IGBT}(t)}{I_N} * (E_{offN} - E_{off0})$$

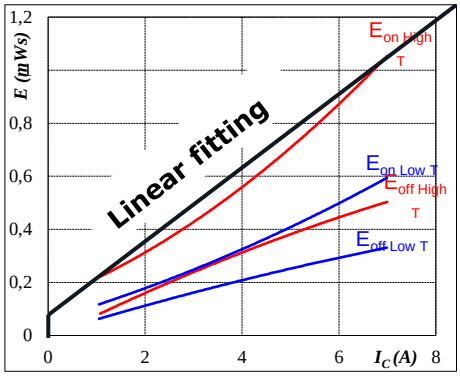


Figure 8:Llinear extrapolation of the energies as a function of switched current

Here:

E_{on0} is the switch-on energy at zero current,

E_{off0} is the switch-off energy at zero current,

E_{onN} is the switch-on energy at nominal current, and

E_{offN} is the switch-off energy at nominal current.

A similar energy loss dependency is assumed as a function of the switched voltage:

$$E_{onIGBT}(I_{IGBT}(t)) = \frac{V_O}{V_N} * \left[E_{on0} + \frac{I_{IGBT}(t)}{I_N} * (E_{onN} - E_{on0})\right] \quad \textbf{(22)}$$

$$E_{offIGBT}(I_{IGBT}(t)) = \frac{V_O}{V_N} * \left[E_{off0} + \frac{I_{IGBT}(t)}{I_N} * (E_{offN} - E_{off0})\right] \quad \textbf{(23)}$$

Here:

V_0 is the switched voltage (half of the output voltage), and

V_N is the voltage level at which E_{onN} and E_{offN} were measured.

Substituting formulas **(22)** and **(23)** in **(21)** and calculating the integral yields the switching losses:

$$P_{sw} = \frac{V_0}{V_N} * f_{sw} * \left[\frac{1}{2} * (E_{on0} + E_{off0}) + \frac{I_{ph(RMS)}}{I_n} * \frac{\sqrt{2}}{\pi} * (E_{onN} + E_{offN} - E_{on0} - E_{off0})\right] \quad \textbf{(24)}$$

4.4.2 Boost free-wheeling diode switching losses

The reverse recovery energy is the source of the fast recovery boost diode's losses. The average switching losses of the fast recovery diode are given by replacing E_{on0}, E_{off0}, E_{onN}, and E_{offN} with E_{rec0} and $Erec_0$.

The average switching losses of the ANPFC boost diode are given by:

$$P_{sw} = \frac{V_0}{V_N} * f_{sw} * \left[\frac{1}{2} * E_{rec0} + \frac{I_{ph(RMS)}}{I_n} * \frac{\sqrt{2}}{\pi} * (E_{recN} - E_{rec0})\right]$$

5 Benchmark of the three-phase PFCs

In this chapter, the operation mode, current loops, and efficiency of the ANPFC topology are compared with other well-established three-level three-phase PFC topologies. Two main categories can be defined. The first category pairs a 600 V switch that commutates with a 600 V FWD. The second category pairs a 600 V switch that commutates with a 1200 V FWD.

The following topologies fall into the first category (600 V switch with a 600 V FWD):

- ANPFC
- SPFC
- Vienna

The remaining topology falls into the second category (600V switch with 1200 V FWD):

- NPFC

Categorising the topologies in terms of their components' breakdown voltages is important to evaluate their switching losses. As the control strategy for all topologies is the same, we can state that, under the same conditions, the switching losses for all 600 V rated topologies are the same when the same components are used. As the only 1200 V rated topology, the NPFC has higher switching losses when using the same current-rated components.

The most well-established and wide-spread three-level PFC topologies are described below:

1. ANPFC

Structure of the ANPFC:

- Two input rectifiers to select the positive and negative input voltages: D43, D44
- Positive and negative side boost switch-diode commutation pairs rated at 600 V: T13-D13 and T14-D14
- A blocking rectifier diode to increase the blocking capability of the positive boost diode: D41

Commutation loops and current paths in the ANPFC topology:

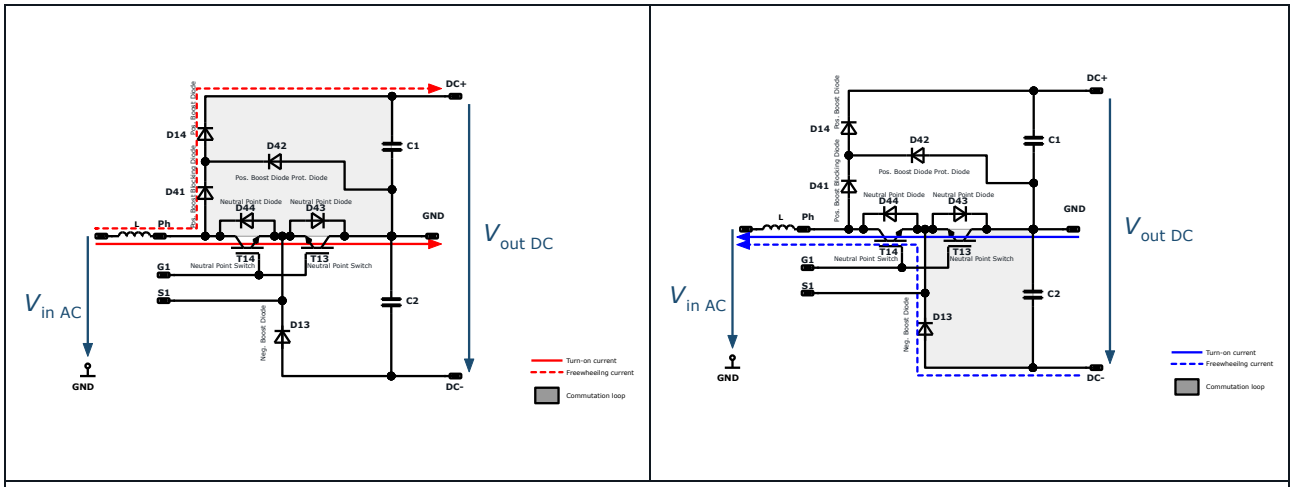


Figure 9: Current paths and commutation loops in the ANPFC topology

Particularity when using MOSFETs instead of IGBTs

If active switches use MOSFETs, the neutral point diode (D43) can be left out. Because the MOSFET's gates are connected when T14 conducts in the forward direction (positive input voltage), channel T13 is also open. T13 conducts in third quadrant with its open channel, eliminating the need for an additional antiparallel rectifier diode.

During the negative input voltage period, when T13 conducts in forward direction and T14 conducts in third quadrant, the situation is the same as in during the positive input period. When T13 is turned off and the current is commutated to the freewheeling diode (D13), channel T14 is closed, resulting in no third-quadrant conduction. Consequently, the freewheeling current must flow through T14 in the reverse direction (Fig. 10).

When the channel T14 is closed, the freewheeling current can only be maintained over the MOSFET body diode. To prevent additional power losses caused by body diode conduction, the rectifier D44 should be retained in the circuit.

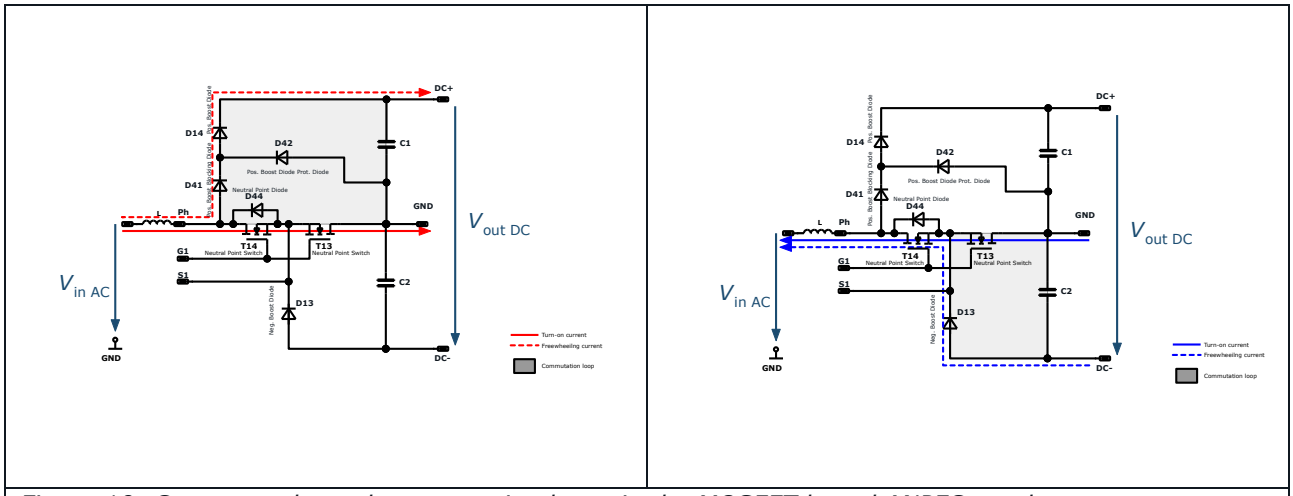


Figure 10: Current paths and commutation loops in the MOSFET based ANPFC topology

2. SPFC – Symmetric PFC

Structure of the SPFC:

- Two input rectifiers to select the positive and negative input voltages: D31, D32
- Positive and negative side boost switch-diode commutation pairs rated at 600 V: T27-D27 and T25-D25

Commutation loops and current paths in the SPFC topology:

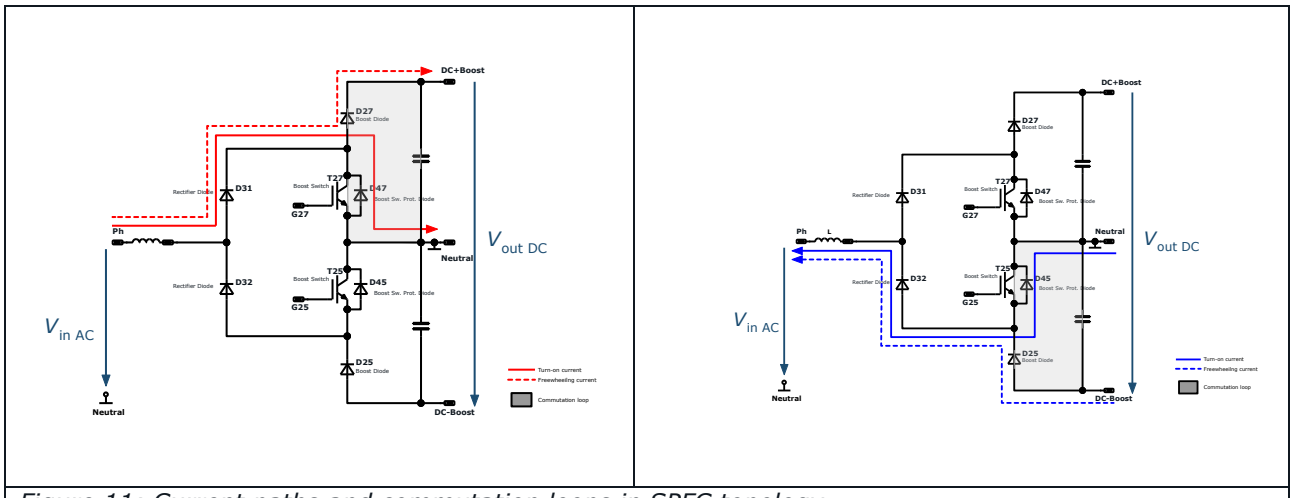


Figure 11: Current paths and commutation loops in SPFC topology

3. NPFC – Neutral point PFC

Structure of the NPFC:

- Two rectifiers to select the positive and negative input voltages: D11, D12
- Positive and negative side boost switch-diode commutation pairs: T13-D13 and T14-D14, where the switch is rated at 600 V and the FWD at 1200 V

Commutation loops and current paths in the NPFC topology:

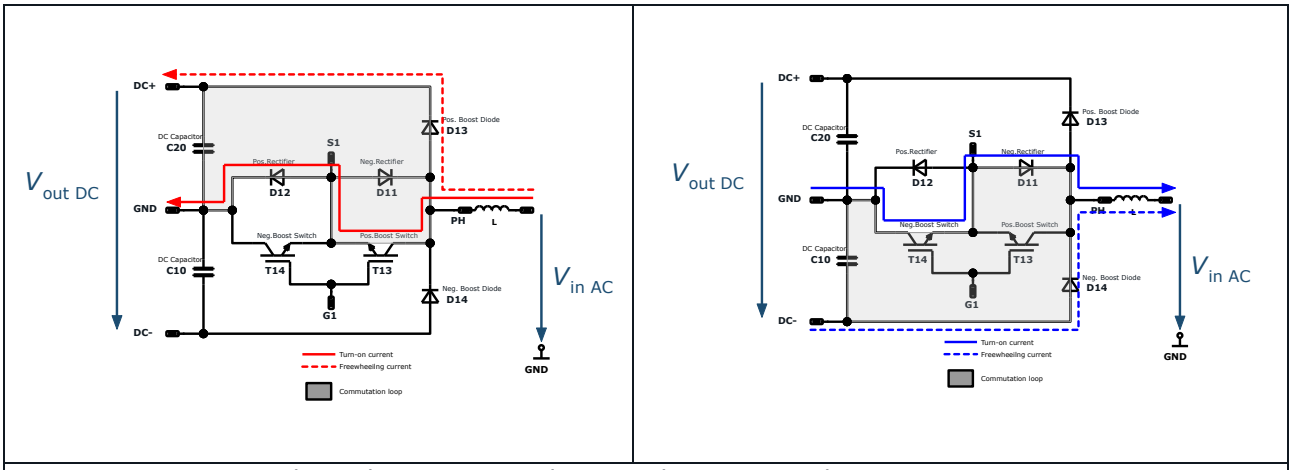


Figure 12: Current paths and commutation loops in the NPFC topology

4. Vienna rectifier

Structure of the Vienna rectifier:

- Two rectifiers to select the positive and negative input voltages: D32, D31
- Positive and negative side boost switch-diode commutation pairs: T15-D15, and T15-D16, where all components are rated at 600 V
- Two rectifier diodes to deliver the energizing current to the neutral GND potential: D33, D34

Commutation loops and current paths in the NPFC topology:

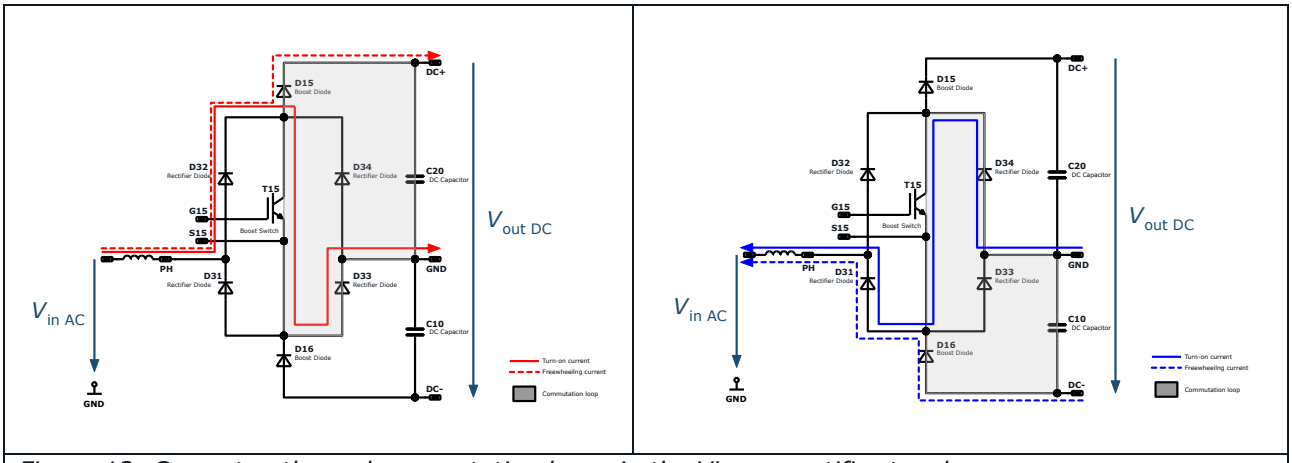


Figure 13: Current paths and commutation loops in the Vienna rectifier topology

5.1 Semiconductor power loss distribution in three-level PFC topologies

As pointed out in the previous section, all three-level topologies feature the following current directions:

- Positive input voltage-current
  - charging current
  - freewheeling current
- Negative input voltage-current
  - charging current
  - freewheeling current

Positive input period loss table:

LOSS DISTRIBUTION							
			Static			Switching	
			IGBT[Duty cycle]	FWD[Duty cycle]	RECT[Duty cycle]	IGBT	FWD
Positive SINE	ANPFC	Charging	$ST_{IGBT}[1-D]$		$ST_{RECT}[1-D]$	SW_{IGBT}	
		Freewheeling		$ST_{FWD}[D]$	$ST_{RECT}[D]$		SW_{FWD}
	SPFC	Charging	$ST_{IGBT}[1-D]$		$ST_{RECT}[1-D]$	SW_{IGBT}	
		Freewheeling		$ST_{FWD}[D]$	$ST_{RECT}[D]$		SW_{FWD}
	NPFC	Charging	$ST_{IGBT}[1-D]$		$ST_{RECT}[1-D]$	SW_{IGBT}	
		Freewheeling		$ST_{FWD}[D]$			SW_{FWD}
	Vienna	Charging	$ST_{IGBT}[1-D]$		$2*ST_{RECT}[1-D]$	SW_{IGBT}	
		Freewheeling		$ST_{FWD}[D]$	$ST_{RECT}[D]$		SW_{FWD}

Negative input period loss table:

LOSS DISTRIBUTION							
			Static			Switching	
			IGBT[Duty cycle]	FWD[Duty cycle]	RECT[Duty cycle]	IGBT	FWD
Negative SINE	ANPFC	Charging	$ST_{IGBT}[1-D]$		$ST_{RECT}[1-D]$	SW_{IGBT}	
		Freewheeling		$ST_{FWD}[D]$	$ST_{RECT}[D]$		SW_{FWD}
	SPFC	Charging	$ST_{IGBT}[1-D]$		$ST_{RECT}[1-D]$	SW_{IGBT}	
		Freewheeling		$ST_{FWD}[D]$	$ST_{RECT}[D]$		SW_{FWD}
	NPFC	Charging	$ST_{IGBT}[1-D]$		$ST_{RECT}[1-D]$	SW_{IGBT}	
		Freewheeling		$ST_{FWD}[D]$			SW_{FWD}
	Vienna	Charging	$ST_{IGBT}[1-D]$		$2*ST_{RECT}[1-D]$	SW_{IGBT}	
		Freewheeling		$ST_{FWD}[D]$	$ST_{RECT}[D]$		SW_{FWD}

$ST_{IGBT}[1-D]$: static losses of a 600 V rated IGBT conducting a current with duty cycle 1-D

$ST_{IGBT}[D]$: static losses of a 600 V rated IGBT conducting a current with duty cycle D

For other components the logic is the same:

$ST_{FWD}[D]$: static losses of a 1200 V component under a duty cycle D

$SW_{IGBT/FWD}$: switching losses of a component rated at 600 V

$SW_{IGBT/FWD}$: switching losses of a component rated at 1200 V

Comparing the loss table line by line yields the following conclusions:

- ANPFC losses are equal to SPFC losses.
- NPFC total loss is lower with one rectifier loss: **$ST_{RECT}[D]$** compared to ANPFC meanwhile contains a 1200 V diode static loss: **$ST_{FWD}[D]$** and two switching losses caused by the 1200 V rated FWD: **SW_{IGBT}, SW_{FWD}**
- The Vienna topology's static losses are higher than the static losses of the ANPFC and of the SPFC with a rectifier loss: **$ST_{RECT}[1-D]$**

5.2 Comparison at a system level

This section examines the gate driver requirements for each topology.

All the topologies using the same switching frequency, choke, and DC link capacitor have the same choke ripple current and holding time.

Gate driver requirements: The ANPFC, NPFC, Vienna topologies require only a single gate driver and a single internal housekeeping DC supply. Meanwhile, the SPFC requires two floating gate drivers, each with its associated internal DC supply.

Loss distribution: The positive (negative) side of the ANPFC, SPFC, NPFC topologies can be associated with the positive (negative) input voltage or current. In the case of the Vienna topology, a single switch is associated with both periods of the input voltage. The Vienna rectifier topology's main switch is subject to higher temperatures for the same application parameters.

5.3 Efficiency comparison

The efficiency comparison of the four topologies was carried out using a 30 A/650 V rated fast IGBT and a 30 A/600 V fast FWD commutation pair for the ANPFC, SPFC, and Vienna topologies. The NPFC commutation pair contains a 30 A/650 V rated fast IGBT and a 35 A/1200 V rated fast FWD.

The rectifier diodes used in all four topologies are rated at 18 A/1600 V.

5.3.1 Efficiency comparison as a function of the input current

The efficiency comparison was carried out under typical application operation conditions:

V_{IN} = 230 V_{AC}

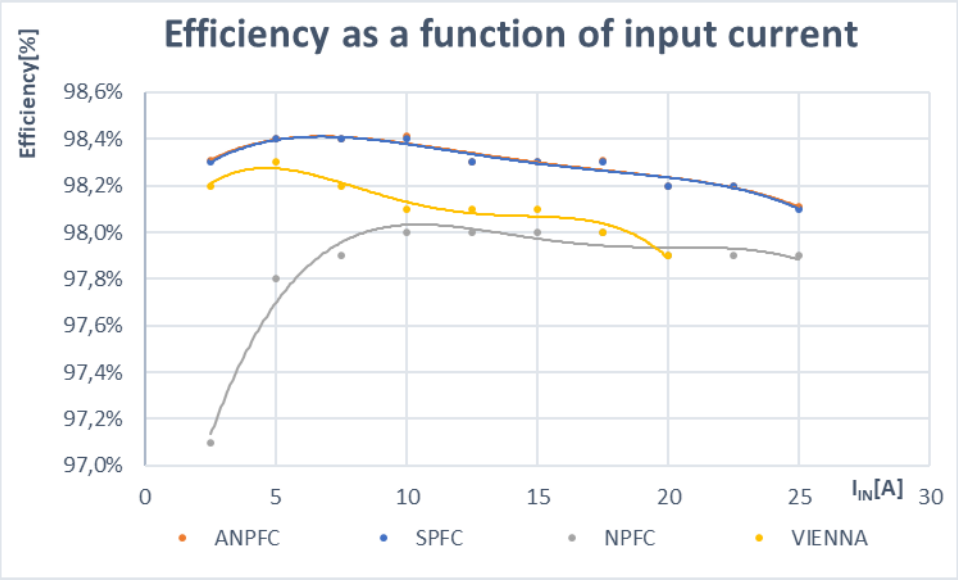
V_{DC} = 800 V

T_H = 80 °C

f_{SW} = 40 Kh

I_{IN} = 2,5…25 A

			eff[%]									
Th=	80 °C	$I_{IN[A]}$	2,5	5	7,5	10	12,5	15	17,5	20	22,5	25
V_{IN} =	230 V_{RMS}	ANPFC	98,31%	98,40%	98,40%	98,41%	98,30%	98,30%	98,31%	98,20%	98,20%	98,11%
V_{DC}=	800 V	SPFC	98,30%	98,40%	98,40%	98,40%	98,30%	98,30%	98,30%	98,20%	98,20%	98,10%
f_{SW}=	40 kHz	NPFC	97,10%	97,80%	97,90%	98,00%	98,00%	98,00%	98,00%	97,90%	97,90%	97,90%
I_{IN}=	2,5-25 A	VIENNA	98,20%	98,30%	98,20%	98,10%	98,10%	98,10%	98,00%	97,90%		



- The ANPFC's efficiency is equal to that of the SPFC with the added benefit of requiring just a single gate driver.
- The efficiencies of the NPFC and Vienna topologies are almost the same. The Vienna rectifier's load capability is limited in comparison to the other three-level topologies. Achieving the same load capability would require a higher current-rated switch in the Vienna rectifier.

5.3.2 Efficiency comparison as a function of the switching frequency

The comparison was carried out at 15 A input current, corresponding to half the current rating of the components. The switching frequencies were swept from 8 to 48 kHz.

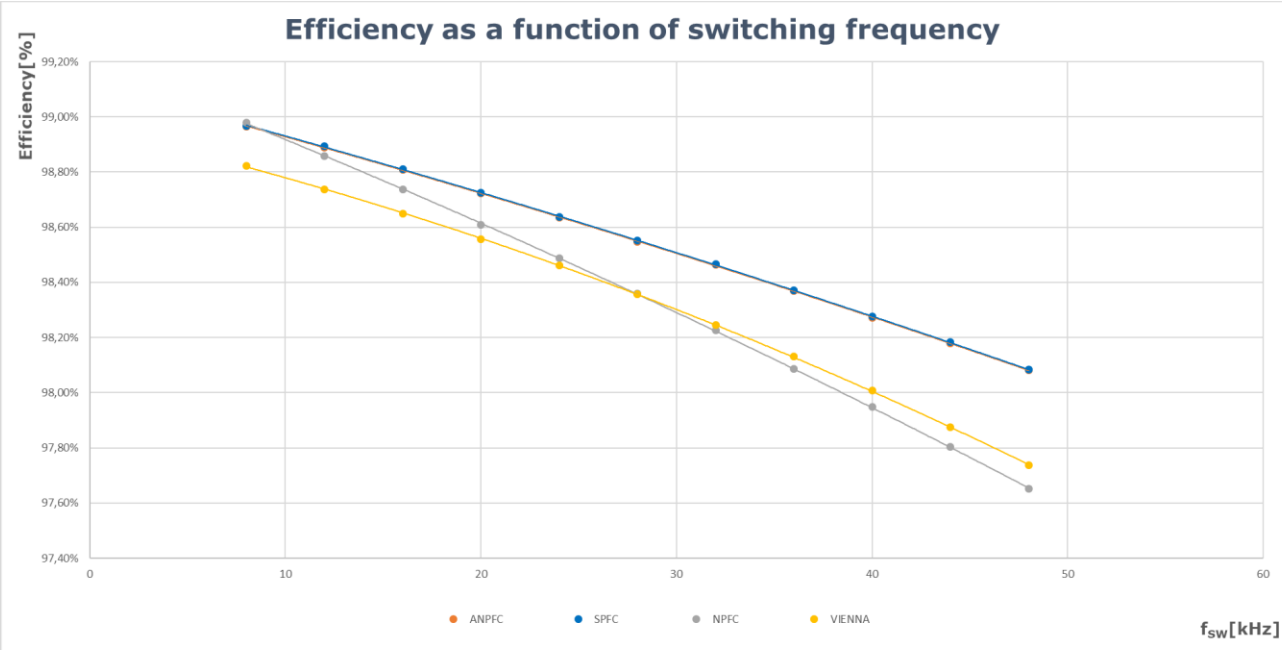
V_{IN} = 230 V_{AC}

V_{DC} = 800 V

T_H = 80 °C

I_{IN} = 15 A

f_{SW} = 8…40 kHz



f_{sw}[kHz]			8				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	2,30	5,6	35,7	98,97%
	FWD		4,80	0,40	5,2		
	RECT	+	2,50		2,5		
		-	7,00		7		
		Block.D	4,60		4,6		
SPFC	IGBT		3,30	2,30	5,60	35,6	98,97%
	FWD		4,80	0,40	5,2		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	2,30	5,60	35,2	98,98%
	FWD		7,80	1,70	9,50		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,50	4,70	11,20	40,6	98,82%
	FWD		4,80	0,40	5,20		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

f_{sw}[kHz]			12				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	3,40	6,70	38,3	98,89%
	FWD		4,80	0,60	5,40		
	RECT	+	2,50		2,50		
		-	7,00		7,00		
		Block.D	4,60		4,60		
SPFC	IGBT		3,30	3,40	6,70	38,2	98,89%
	FWD		4,80	0,60	5,4		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	3,60	6,90	39,4	98,86%
	FWD		7,80	2,50	10,30		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,50	7,30	13,80	43,6	98,74%
	FWD		4,80	0,60	5,40		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

f_{sw}[kHz]			16				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	4,60	7,90	41,1	98,81%
	FWD		4,80	0,80	5,60		
	RECT	+	2,50		2,50		
		-	7,00		7,00		
		Block.D	4,60		4,60		
SPFC	IGBT		3,30	4,60	7,90	41,0	98,81%
	FWD		4,80	0,80	5,6		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	4,80	8,10	43,6	98,74%
	FWD		7,80	3,40	11,20		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,50	9,90	16,40	46,6	98,65%
	FWD		4,80	0,80	5,60		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

f_{sw}[kHz]			20				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	5,90	9,20	44,1	98,72%
	FWD		4,80	1,00	5,80		
	RECT	+	2,50		2,50		
		-	7,00		7,00		
		Block.D	4,60		4,60		
SPFC	IGBT		3,30	5,90	9,20	44,0	98,72%
	FWD		4,80	1,00	5,8		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	6,10	9,40	48,0	98,61%
	FWD		7,80	4,30	12,10		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,50	12,70	19,20	49,8	98,56%
	FWD		4,80	1,00	5,80		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

f_{sw}[kHz]			24				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	7,20	10,50	47,1	98,63%
	FWD		4,80	1,20	6,00		
	RECT	+	2,50		2,50		
		-	7,00		7,00		
		Block.D	4,60		4,60		
SPFC	IGBT		3,30	7,20	10,50	47,0	98,64%
	FWD		4,80	1,20	6		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	7,30	10,60	52,2	98,49%
	FWD		7,80	5,20	13,00		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,50	15,60	22,10	53,1	98,46%
	FWD		4,80	1,20	6,00		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

f_{sw}[kHz]			28				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	8,50	11,80	50,1	98,55%
	FWD		4,80	1,40	6,20		
	RECT	+	2,50		2,50		
		-	7,00		7,00		
		Block.D	4,60		4,60		
SPFC	IGBT		3,30	8,50	11,80	50,0	98,55%
	FWD		4,80	1,40	6,2		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	8,65	11,95	56,6	98,36%
	FWD		7,70	6,15	13,85		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,60	18,70	25,30	56,7	98,36%
	FWD		4,80	1,40	6,20		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

f_{sw}[kHz]			32				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	9,75	13,05	53,0	98,46%
	FWD		4,80	1,60	6,40		
	RECT	+	2,50		2,50		
		-	7,00		7,00		
		Block.D	4,60		4,60		
SPFC	IGBT		3,30	9,75	13,05	52,9	98,47%
	FWD		4,80	1,60	6,4		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	9,95	13,25	61,2	98,23%
	FWD		7,70	7,15	14,85		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,60	22,10	28,70	60,5	98,25%
	FWD		4,80	1,60	6,40		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

f_{sw}[kHz]			36				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	11,15	14,45	56,3	98,37%
	FWD		4,80	1,85	6,65		
	RECT	+	2,50		2,50		
		-	7,00		7,00		
		Block.D	4,60		4,60		
SPFC	IGBT		3,30	11,15	14,45	56,2	98,37%
	FWD		4,80	1,85	6,65		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	11,35	14,65	66,0	98,09%
	FWD		7,70	8,15	15,85		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,60	25,60	32,20	64,5	98,13%
	FWD		4,80	1,85	6,65		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

f_{sw}[kHz]			40				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	12,55	15,85	59,6	98,27%
	FWD		4,80	2,10	6,90		
	RECT	+	2,50		2,50		
		-	7,00		7,00		
		Block.D	4,60		4,60		
SPFC	IGBT		3,30	12,55	15,85	59,5	98,28%
	FWD		4,80	2,10	6,9		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	12,75	16,05	70,8	97,95%
	FWD		7,70	9,15	16,85		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,60	29,30	35,90	68,7	98,01%
	FWD		4,80	2,10	6,90		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

f_{sw}[kHz]			44				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	13,95	17,25	62,8	98,18%
	FWD		4,80	2,30	7,10		
	RECT	+	2,50		2,50		
		-	7,00		7,00		
		Block.D	4,60		4,60		
SPFC	IGBT		3,30	13,95	17,25	62,7	98,18%
	FWD		4,80	2,30	7,1		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	14,15	17,45	75,8	97,80%
	FWD		7,70	10,25	17,95		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,60	33,50	40,10	73,3	97,88%
	FWD		4,80	2,30	7,10		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

f_{sw}[kHz]			48				
			P_{STATIC}[W]	$P_{SWITCHING}$[W]	P_{TOT}[W]	P_{TOT_MODULE}[W]	E_{ff}[%]
ANPFC	IGBT		3,30	15,45	18,75	66,2	98,08%
	FWD		4,80	2,50	7,30		
	RECT	+	2,50		2,50		
		-	7,00		7,00		
		Block.D	4,60		4,60		
SPFC	IGBT		3,30	15,45	18,75	66,1	98,08%
	FWD		4,80	2,50	7,3		
	RECT	+	7,00		7		
		-	7,00		7		
NPFC	IGBT		3,30	15,65	18,95	81,0	97,65%
	FWD		7,70	11,35	19,05		
	RECT	+	2,50		2,5		
		-	2,50		2,5		
VIENNA	IGBT		6,60	37,90	44,50	78,1	97,74%
	FWD		4,80	2,50	7,30		
	RECT	INPUT	7,00		7		
		GND	2,5		2,5		

6 Conclusion

The application note describes the ANPFC topology. Starting from the circuit composition, it highlights the innovative topology’s key features. Benchmark key characteristic of ANPFC are implemented, comparing against other conventional three-phase three-level PFC circuits. The advantages of the ANPFC topology over other well-established three-level topologies can be summarized as follows:

- Because the ANPFC uses a single gate driver and components rated at 600 V, it achieves the highest efficiency and is cost-effective.
- The ANPFC has a uniform loss distribution among its components.

- The ANPFC's modulation and control scheme is identical to all other three-level PFC topologies, enabling a fast transition from standard topologies to the ANPFC solution.