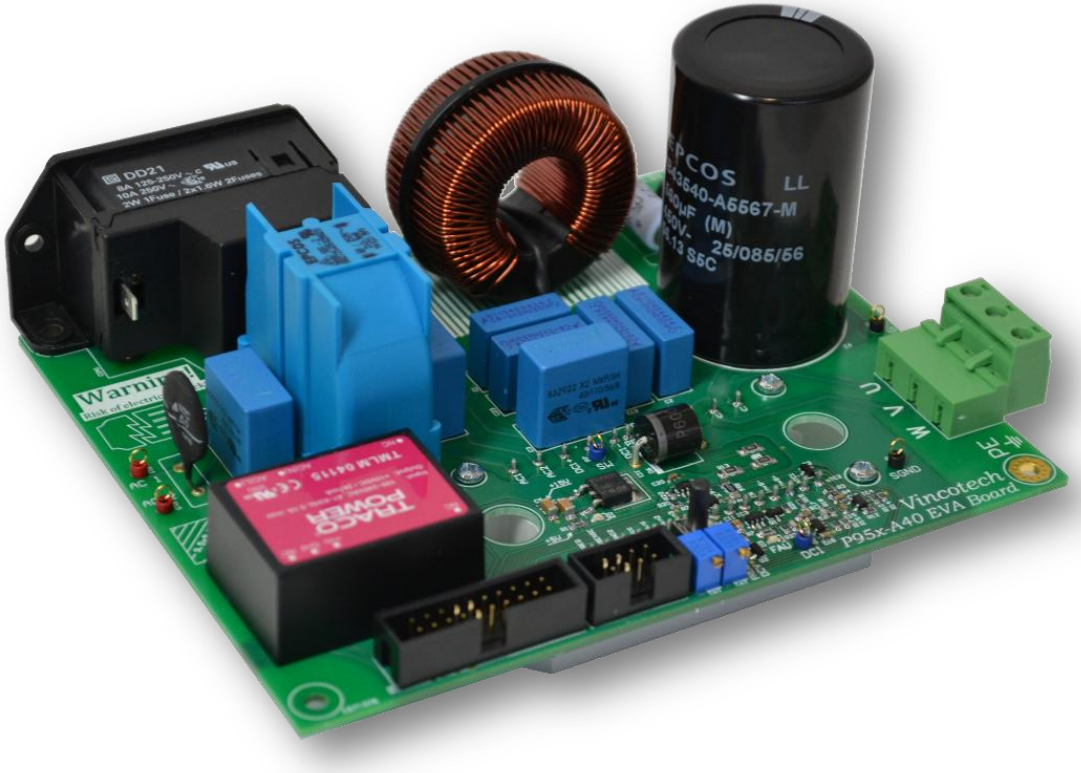
Vincotech

Reference Design for IPM Modules

Evaluation Board for P95X-A40 TF IPM Modules with an Integrated PFC Controller



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Revision History

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2015 - Mar	1	First release	42
2016 - Jan	2	Fig. 24-25 corrected	42

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1 Introduction

Safety Information

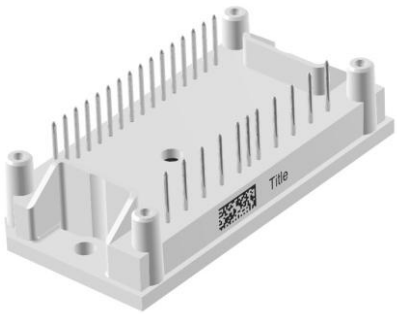
*The board described herein is an evaluation board (EVA board) designed for laboratory environments only. It operates at high voltages and **must** be operated only by qualified and skilled personnel familiar with all applicable safety standards.*
Caution: This EVA board can endanger lives by exposing people to rotating machinery and high voltages. Its ground potential is not floating; it is biased to the negative DC link voltage potential. Use an isolation transformer at the AC input to take measurements with a non-floating instrument (oscilloscope). Allow at least two minutes to elapse for the DC link capacitor to discharge to safe voltage levels (< 50 V). Use an insulated screw driver to set the switching frequency or DC link voltage. Failure to heed these guidelines may result in personal injury or death and/or equipment damage.

1.1 Abstract

This application note describes the Evaluation Driver Board for the P95x-A40 family of thick-film integrated power modules. To learn more about Vincotech modules, please visit www.vincotech.com. This board provides a plug-and-play solution for identifying this family of module's switching behavior and efficiency.

1.2 A brief introduction to P95x-A40 thick-film IPMs

The P955-A40 and P952-A40 are thick-film (TF) integrated power modules (IPM) designed for small motion control applications. Housed in *flow*IPM 1B chassis, they are excellent choices for compact applications such as embedded motor drives for fans, pumps, washing machines and small industrial motor drives.



These modules contain all the requisite high-voltage, high-power electronic components (input rectifier, PFC, PFC-shunt, six-pack inverter, DC shunt, DC capacitor), gate drivers and a CCM PFC controller with feedback networks and compensation.

Key components:

- Complete high-voltage electronic circuit from a single-phase AC input (85 to 264 V_{RMS}) to a three-phase AC output
- An integrated PFC controller with programmable DC bus voltage (325 V to 400 V) and programmable switching frequency (20 kHz to 100 kHz)
- Under-voltage, over-current and shoot-through protection for the inverter stage
- Integrated shunt resistor for measuring the DC bus current
- Integrated NTC thermistor for measuring the substrate temperature

Figure 1 is a streamlined block diagram of the motor control system with a single-phase input routed to a three-phase output.

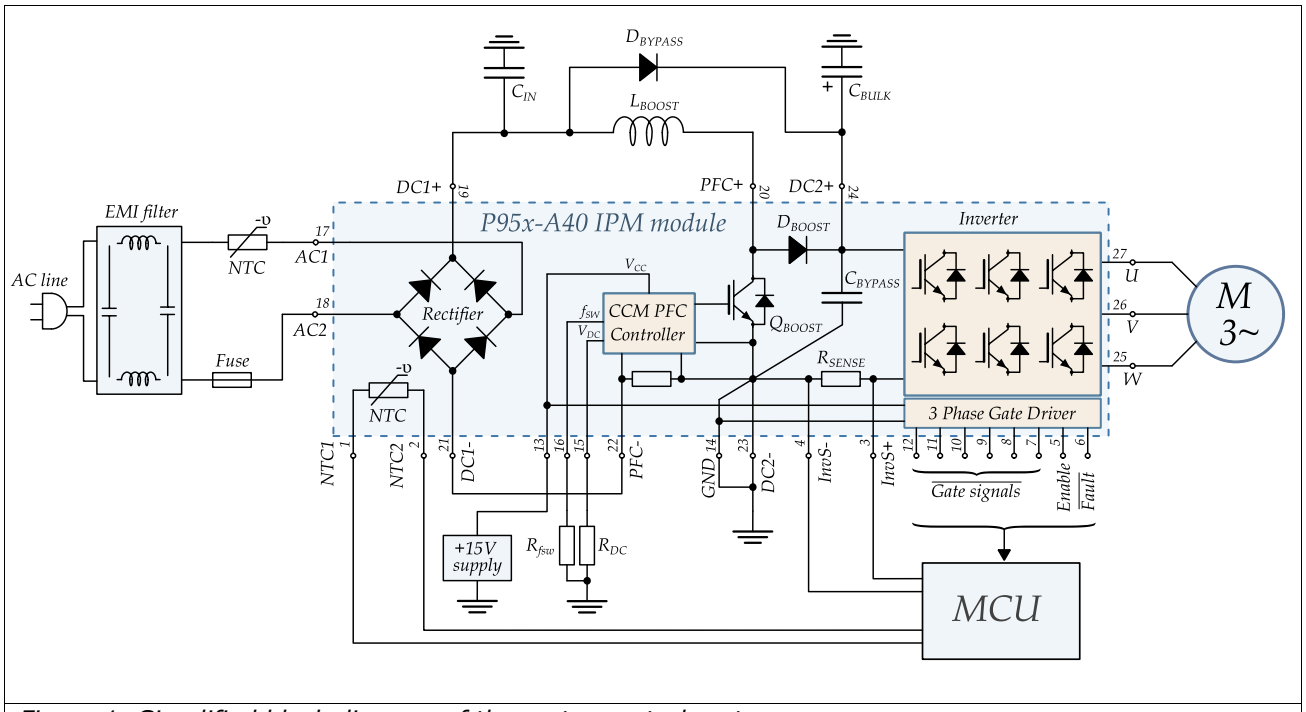
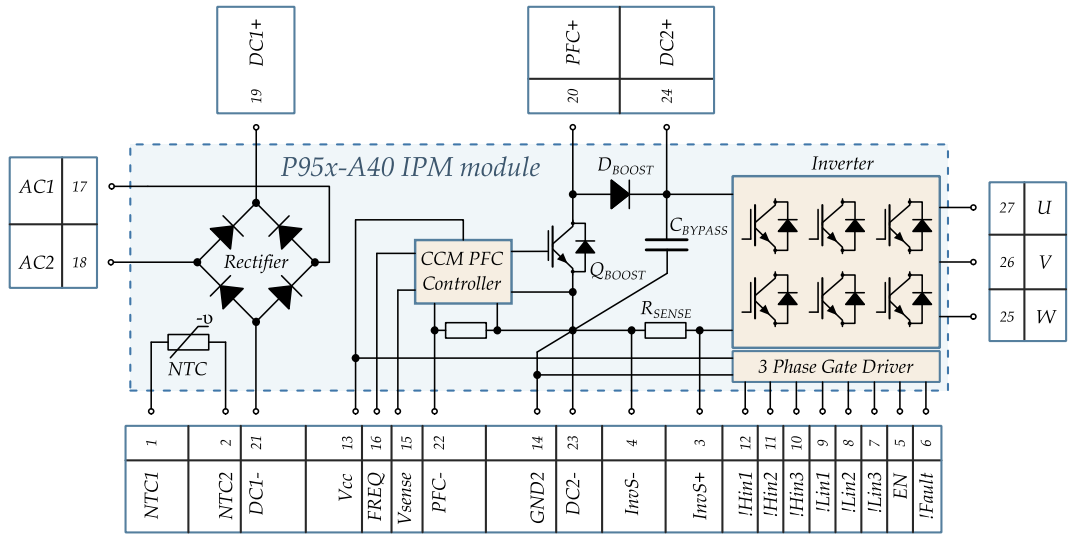
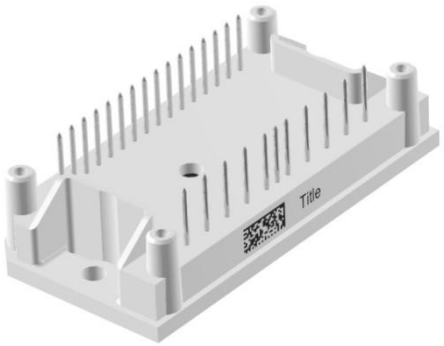
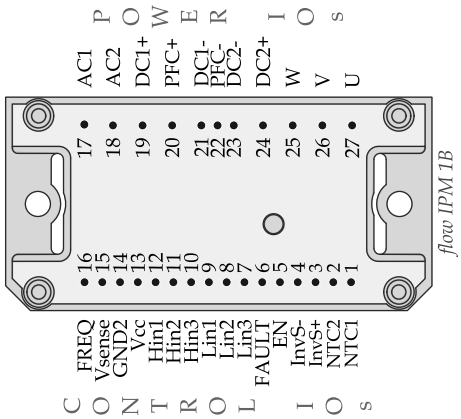


Figure 1: Simplified block diagram of the motor control system







Pin #	Pin Name	Pin Description	Pin #	Pin Name	Pin Description
1	NTC1	NTC thermistor pin 2	15	Vsense	PFC output voltage programming
2	NTC2	NTC thermistor pin 1	16	FREQ	PFC switching frequency programming
3	InvS+	Inverter shunt resistor high-side	17	AC1	Rectifier input 1
4	InvS-	Inverter shunt resistor low-side	18	AC2	Rectifier input 2
5	EN	Inverter enable	19	DC1+	Rectifier output +
6	$\overline{\text{Fault}}$	Inverter fault	20	PFC+	PFC switched node
7	$\overline{\text{Lin 3}}$	Low-side logic input (Phase U)	21	DC1-	Rectifier output -
8	$\overline{\text{Lin 2}}$	Low-side logic input (Phase V)	22	PFC-	PFC return
9	$\overline{\text{Lin 1}}$	Low-side logic input (Phase W)	23	DC2-	Inverter input DC-
10	$\overline{\text{Hin 3}}$	High-side logic input (Phase U)	24	DC2+	Inverter input DC+
11	$\overline{\text{Hin 2}}$	High-side logic input (Phase V)	25	W	Phase W output

12	$\overline{\text{Hin 1}}$	High-side logic input (Phase W)	26	V	Phase V output
13	Vcc	Inverter and PFC +15 V power supply	27	U	Phase U output
14	GND2	Logic and analog ground			

1.3 An introduction to the EVA board

- Suitable for P95x-A40 family
- Single-phase, 85 V_{AC} – 264 V_{AC} input voltage
- Onboard EMI filter, fuse, NTC inrush protection
- Complete solution for a 1 kW , three-phase motor drive application
- DC link voltage and switching frequency adjustable via trimmer potentiometer
- Onboard 15V power supply for an integrated PFC controller and gate driver circuit
- 5V TTL-compatible control I/Os
- Enabled input for the inverter stage (active high)
- Fault output signal from the inverter stage (active low)

1.4 Circuitry

The EVA board's power stage is a conventional six-pack inverter connected to the boost PFC converter's output. The PFC stage consists of a rectifier bridge, boost inductor, high-speed IGBT, boost diode and C4 output capacitor.

The boost diode does not handle surge current well, so the D1 bypass diode is on board to protect it against surge current at startup. The D6 diode serves the same purpose for the thick-film PFC sense resistor, protecting it against surge current at startup.

The input stage consists of an IEC C14 appliance inlet connector with a two-pole line switch and a 6.3 A anti-surge (T) fuse followed by an inrush current-limiting NTC thermistor.

The EVA board is equipped with an input EMI filter to meet EMC standards. It cuts switching noise emitted by the boost and inverter stage.

The R3, R4 resistive divider connected to the NTC integrated in the P95x-A40 provides a TEMP signal that is inversely proportional to the substrate temperature. The board is equipped with protection circuits such as over-temperature, over-voltage and over-current. In the event of a fault, the protection circuits shut down the output inverter section and the fault latch circuit stores the fault state. The red D3 LED indicates the fault condition. The user can reset the fault by pressing the B1 button or addressing a reset pulse to pin 5 on the P2 connector.

The shunt resistor integrated in the P95x-A40 serves to sense motor current. The current measurement circuit connected to this current signal provides sufficient gain and offset for easy interfacing with an A/D converter. The PFC switching frequency and DC link voltage can

be programmed via the P3, P4 potentiometers. The DC link voltage is measured directly using the resistive dividers (R8, R11, R13 and R16).

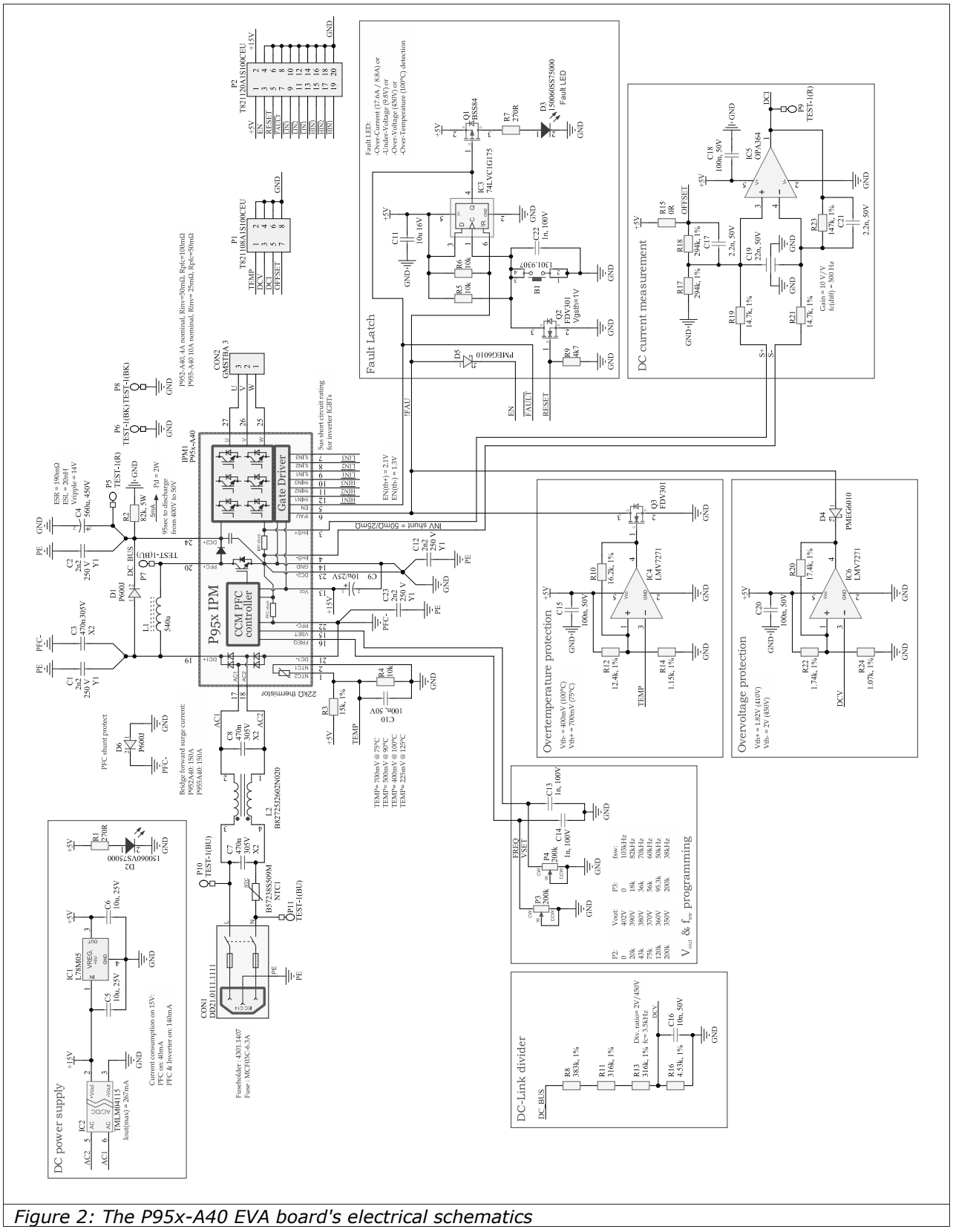


Figure 2: The P95x-A40 EVA board's electrical schematics

1.5 Hardware

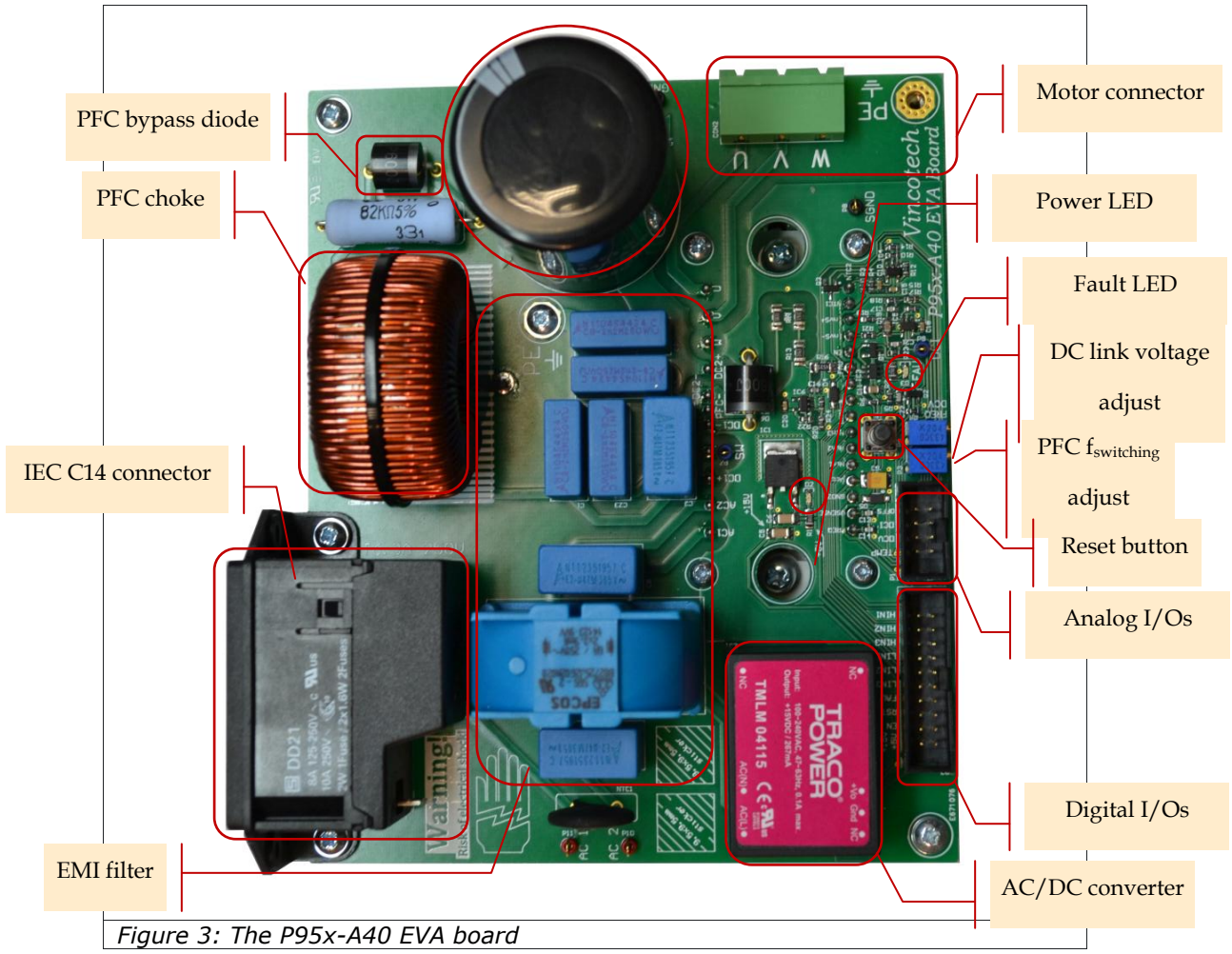


Figure 3: The P95x-A40 EVA board

The recommended heatsink for testing is the Fischer Elektronik type SK47. Apply thermal conductive paste between the P95x-A40 and heatsink with a thickness not exceeding 50 µm. Use M4 screws to fasten the module to the heatsink with 2.0 to 2.2 Nm mounting torque.

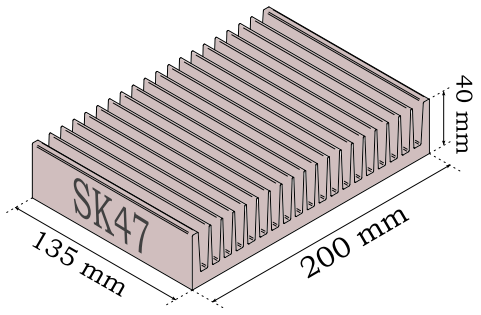


Figure 4: Recommended heatsink

1.6 Switching frequency and DC link voltage programming

The P95x-A40 is able to set the PFC stage switching frequency and DC link voltage via external resistors. The P3 potentiometer may be used to adjust the PFC switching frequency and the P4 potentiometer to adjust the DC link voltage.

The switching frequency may be adjusted within a range of 38 kHz to 100 kHz and the DC link voltage from 350 V to 400 V.

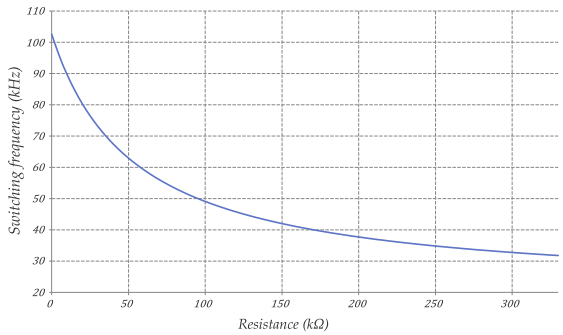


Figure 5: PFC switching frequency as a function of external resistance

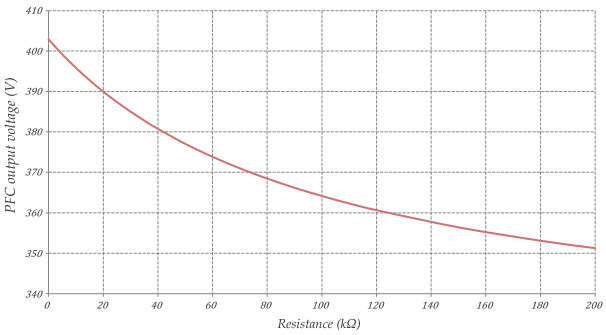


Figure 6: DC link voltage as a function of external resistance

For safety reasons, use an insulated screw driver to set the switching frequency or DC link voltage.

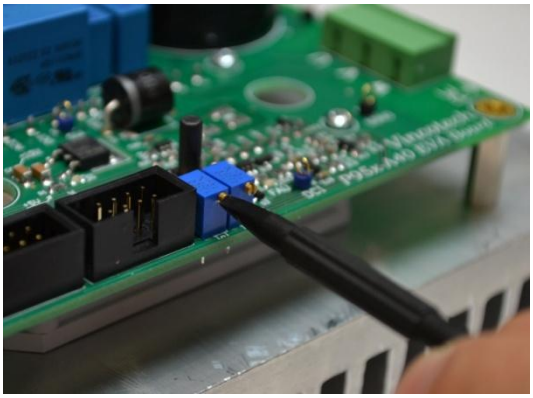


Figure 7: Adjusting the switching frequency with an insulated screwdriver

The P2 and P1 connectors are the interfaces to the P95x-A40 EVA board. The P2 connector taps a group of digital signals such as inverter low-side and high-side PWM control signals through Lin 1 to Lin3 and Hin 1 to Hin 3, $\overline{\text{Fault}}$ output, inverter ENable and Fault reset.

The P1 connector taps a group of analog signals such as the TEMP substrate temperature signal, the DCV DC link voltage signal, the DCI motor current signal and the OFFSET input, which shifts the DCI output with an applied voltage.

The figure and tables below show how the connector P2 and P1's signals are mapped.

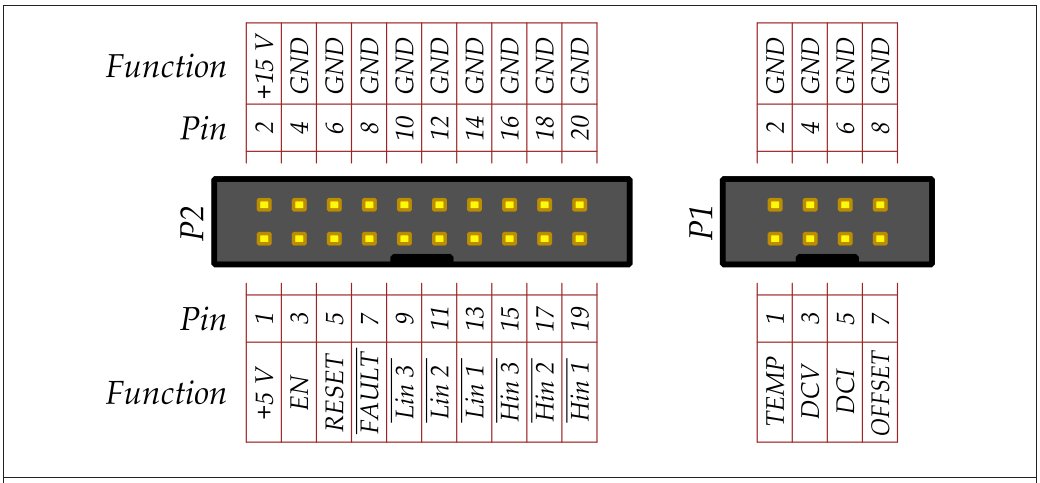


Figure 8: A map of the P2 and P1 connectors' pins

Pin	Function	Direction	Description
1	+5 V	Power output	+5 V, 100 mA output
2	+15 V	Power output	+15 V, 100 mA output
3	EN	Logic input	Inverter enable
5	RESET	Logic input	Fault reset
7	$\overline{\text{Fault}}$	Logic output	$\overline{\text{Fault}}$ output
9	$\overline{\text{Lin 3}}$	Logic input	Inverter low side PWM
11	$\overline{\text{Lin 2}}$	Logic input	Inverter low side PWM
13	$\overline{\text{Lin 1}}$	Logic input	Inverter low side PWM
15	$\overline{\text{Hin 3}}$	Logic input	Inverter high side PWM
17	$\overline{\text{Hin 2}}$	Logic input	Inverter high side PWM
19	$\overline{\text{Hin 1}}$	Logic input	Inverter high side PWM
Remained	GND	Reference	Ground

Table 2: The P2 connector's pin assignments

Pin	Function	Direction	Description
1	TEMP	Analog output	Temperature signal
3	DCV	Analog output	DC link voltage signal
5	DCI	Analog output	Motor current signal
7	OFFSET	Analog input	DCI output offset
Remained	GND	Reference	Ground

Table 1: The P1 connector's pin assignments

The inverter low-side and high-side control pins have a Schmitt-trigger negative logic input with an internal pull-up of 75 kΩ to the +15 V supply rail.

The P95x family provides shoot-through prevention to ensure two channels of the same leg are on at the same time. A minimum dead-time insertion of 310 ns serves to reduce cross-conduction of the IGBT power switch.

The signal applied to the EN pin controls the inverter stage. The inverter is disabled when EN is at the 'low' logic level. The EN pin's typical propagation delay time Pin is 800 ns. The $\overline{\text{Fault}}$ pin indicates the inverter stage's status. This pin's status is low when the following conditions are given:

- Under-voltage at the +15 V supply (sensed by the inverter gate driver)
- Motor over-current detected (over-current protection circuit)
- Over-temperature detected on the substrate (over-temperature protection circuit)
- Over-voltage detected at the DC link (over-voltage protection circuit)

For more details on P1connector pins, refer to section covering analog circuits.

1.8 Operation

Once an external power source meeting the input voltage specification is routed to the EVA board, the PFC stage will run automatically and the inverter stage is automatically disabled. The PFC stage uses a soft-start to reduce the inrush current at startup. Typical settling time during a soft-start is 200 ms.

After the DC link voltage has been set, the user should enable the inverter stage with a reset pulse of at least 1 µs at the RESET input or by pressing the B1button. The inverter stage is enabled 800 ns beyond the reset pulse's falling edge, after which the module can handle PWM signals. The recommended switching frequency for the inverter stage is 16 kHz.

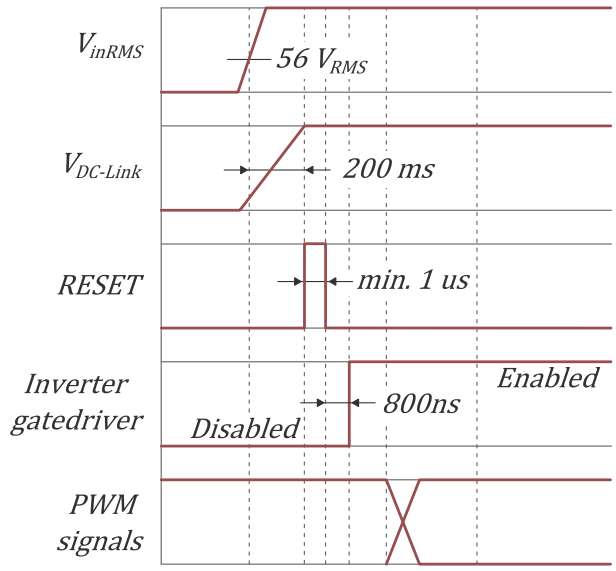


Figure 9: Timing

1.9 Electrical parameters

The electrical parameters are indicated as a guaranteed value range for the supply voltages, load and junction temperature as given below. Typical values are median and given in the context of production processes. Unless otherwise noted, all voltages are indicated with respect to their ground (GND).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
AC input voltage	$V_{AC,IN}$	85	230	264	V_{RMS}	f_{in}=47-63 Hz
AC input current	I_{IN}			5.5	A_{RMS}	f_{PWM}=100 kHz
DC link voltage	V_{DC}	350		400	V_{DC}	internally limited
Inverter AC output voltage	$V_{OUT,AC}$			230	V_{AC}	400V DC link SPWM modulation
AC output current	$I_{OUT,AC}$			3.5	A_{RMS}	
PFC switching frequency	$f_{SW,PFC}$	38		100	kHz	internally limited
EN input logic high	$V_{EN,TH+}$	3.3			V	Inverter enabled
EN input logic low	$V_{EN,TH-}$			1.7	V	Inverter disabled
RESET input logic high	$V_{RST,TH+}$	2.7			V	
RESET input logic low	$V_{RST,TH-}$			0.5	V	
$\overline{\text{FAULT}}$ output high	$V_{FLT,OH}$	4.9			V	I_{OH}=-100 µA
$\overline{\text{FAULT}}$ output low	$V_{FLT,OL}$			0.1	V	I_{OL}=100 µA
$\overline{\text{LINx}}$, $\overline{\text{HINx}}$ input high	$V_{IN,H}$	1.7	2.1	2.4	V	75 kΩ pull-up
$\overline{\text{LINx}}$, $\overline{\text{HINx}}$ input low	$V_{IN,L}$	0.7	0.9	1.1	V	75 kΩ pull-up
TEMP output	V_{TEMP}	0		2	V	
DCV output	V_{DCV}	0		2	V	2 V @ 450 V DC link
DCI output	V_{DCI}	0	2.5	5	V	
OFFSET input	V_{OFFSET}	0	2.5	5	V	

Table 3: The P955-A40 EVA board's electrical parameters

2 PFC converter design

2.1 Target specification

Parameter	Min.	Typ.	Max.	Unit	Remarks
AC input voltage range	85		264	V_{AC}	
AC input line frequency	47		63	Hz	
Nominal DC output voltage		400		V_{DC}	User can adjust DC link voltage, but the PFC stage is designed for 400 V_{DC} output
Maximum output power			1000	W	@ V_{in}=200 $V_{AC,RMS}$, see figure 10.
			500	W	@ V_{in}=100 $V_{AC,RMS}$, see figure 10.
Minimum output holdup time		20		ms	@ $V_{out(min)}$=300 V_{DC}
Switching frequency			100	kHz	User can adjust switching frequency, but the PFC converter is designed for 100 kHz

Table 4: Target specification

This design uses the P955-A40's maximum input current handling capacity to specify the maximum output power. Therefore, the maximum output power $P_{out(max)}$ is proportional to the input voltage V_{in} times the module's maximum input current capability $I_{in(max)RMS}$.The P955-A40's input current handling capacity is 5.5 A, so the module can achieve 1000 W output power at 200 $V_{AC(RMS)}$ input voltage:

$$P_{out(max)} = I_{in(max)RMS} * V_{in(RMS)} * \eta_{min} = 5.5\,A * 200\,V * 0.94 = 1000\,W$$

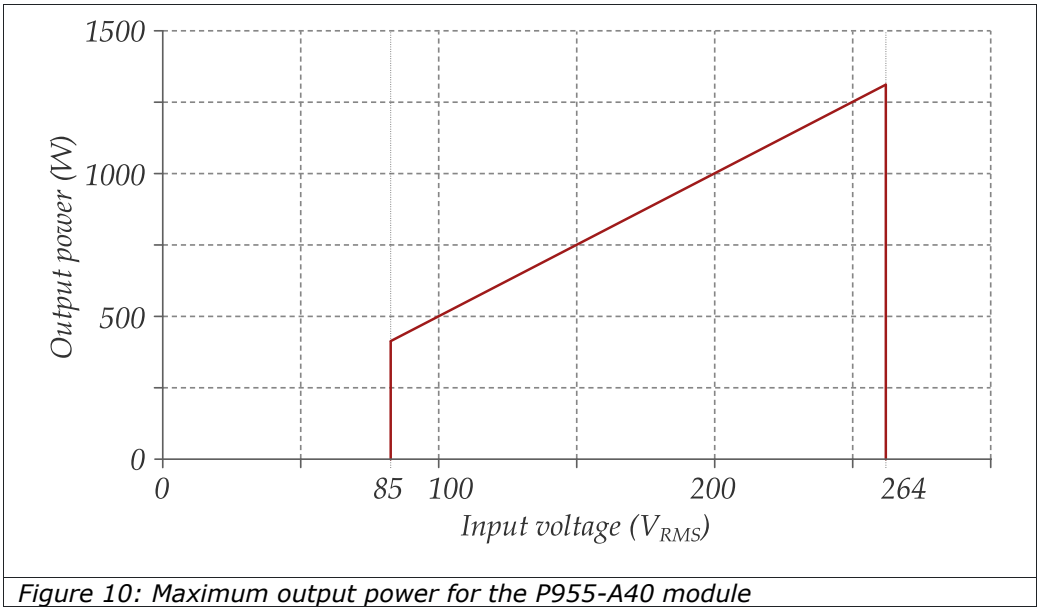


Figure 10: Maximum output power for the P955-A40 module

With a worldwide input voltage specification (85 V-264 V), the module can provide 425 W output power at any (specified) input voltage.

The PFC stage supports a boost topology and operates in continuous conduction mode.

Figure 11 shows a typical inductor current. The inductor must carry the sum of the average inductor current $I_{L(AVG)}$ (which is equal to the input current) and the ripple current (ΔI_L).

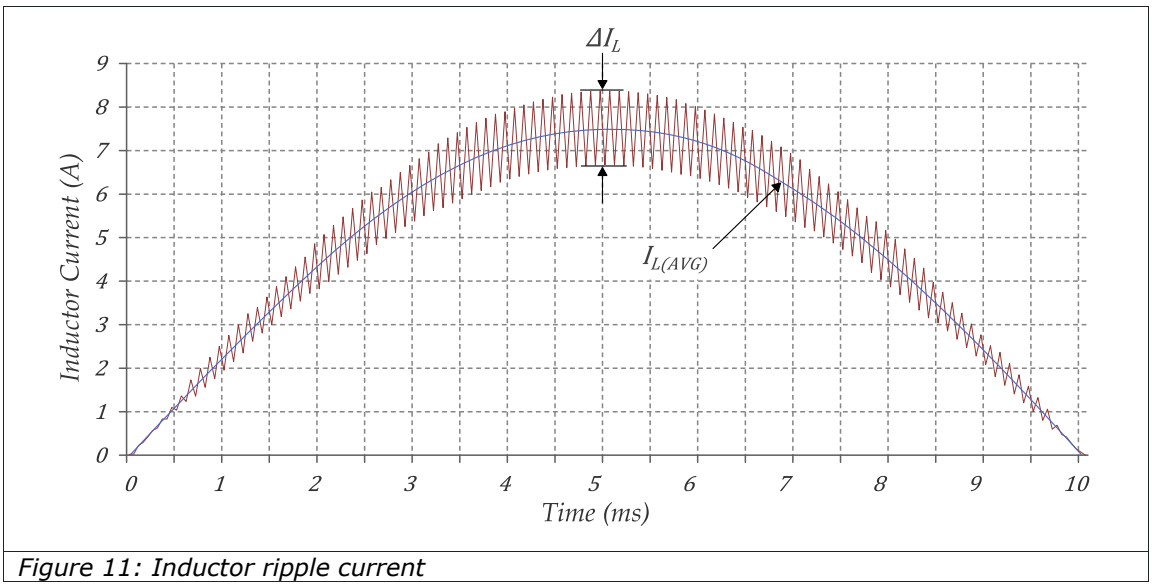


Figure 11: Inductor ripple current

The ripple factor (k_{RF}) is the ratio between the inductor ripple current and average input current at the peak line voltage. The ripple factor vs. input voltage function attains its maximum value where the line voltage peak is equal to half of the output voltage. At 400 V_{DC} DC link voltage, the ripple factor attains its maximum value:

$$V_{in(RMS)} = \frac{V_{out}}{2} = \frac{400\ V_{DC}}{2} = 200\ V_{pk} = 141\ V_{RMS}$$

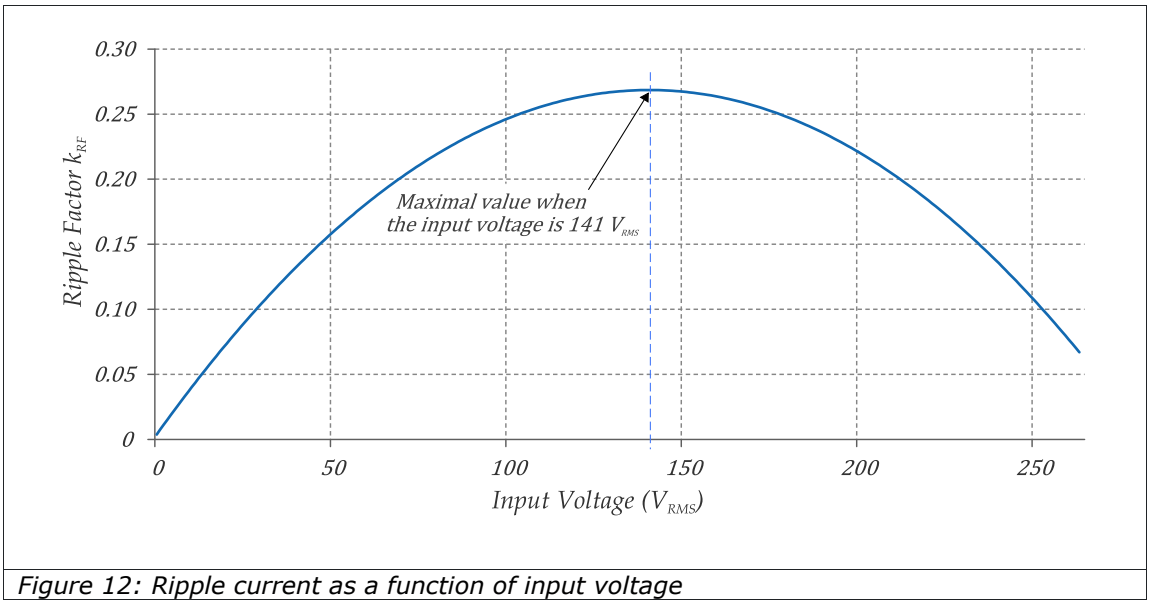


Figure 12: Ripple current as a function of input voltage

The following figures show the inductor current and ripple current at various input voltages.

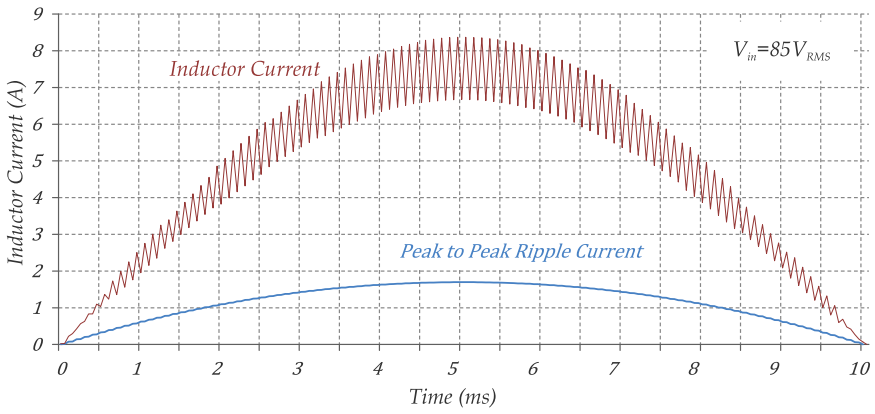


Figure 13: Inductor current at 85 V input voltage

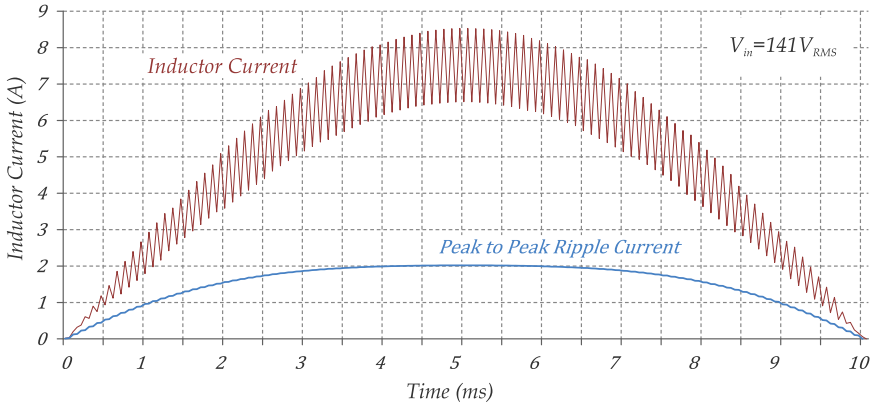


Figure 14: Inductor current at 141 V input voltage

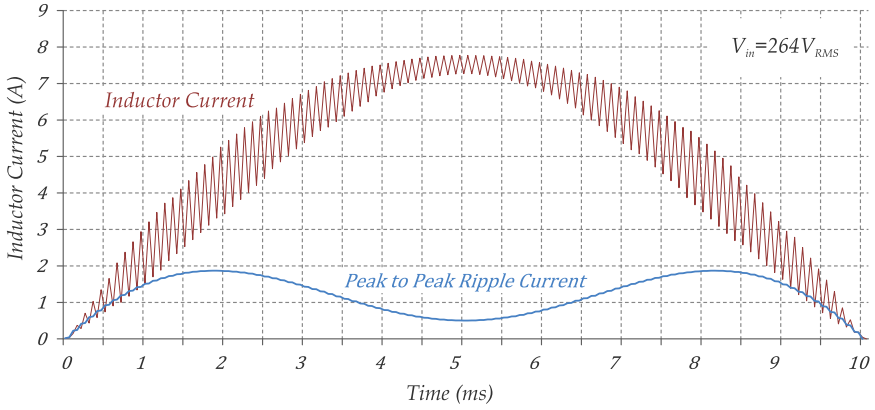


Figure 15: Inductor current at 264 V input voltage

A lower ripple factor reduces distortion, the DC link capacitor ripple current at f_{sw}, peak current in the power switch and the EMI level, but size and cost increase as a result.

A lower ripple factor also reduces inductor core hysteresis loss, which is proportional to the area under the peak-to-peak ripple current in a half-period.

2.2 Boost inductor design

The selected inductor ripple factor is 27%. The ripple current at peak input current is:

$$I_{in(peak)} = \sqrt{2} * I_{in(max)RMS} = 7.77\ A$$
$$\Delta I_L = 27\ \% * I_{in(peak)} = 2.1\ A$$

The peak inductor current is:

$$I_{L(max)} = I_{in(peak)} + \frac{\Delta I_L}{2} = 7.77\ A + \frac{2.1\ A}{2} = 8.82\ A$$

The boost choke inductance must be greater or equal to:

$$L_{Boost} \geq \frac{D * (1 - D) * V_{out(DC)}}{\Delta I_L * f_{SW}}$$

The above equation attains its maximum value with D=0.5 (duty cycle)

$$L_{Boost} \geq \frac{0.5^2 * 400\ V}{2.1\ A * 100\ kHz} = 476\ \mu H$$

The selected core is a Hitachi Metals Microlite MP4010MPFC. It can operate at high DC bias and is cost effective. The table below lists the core's parameters:

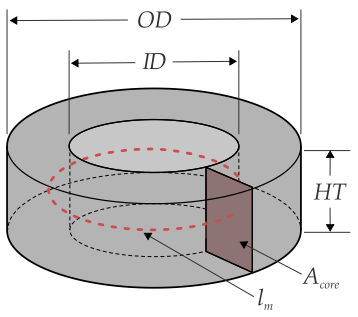
$l_m = 9.76\ cm$	$A_{\mathrm{L}} = 94\ \frac{\mathrm{nH}}{\mathrm{N}^2}$	
$A_{\mathrm{core}} = 0.73\ \mathrm{cm}^2$	$B_{\mathrm{sat}} = 1.56\ \mathrm{T}$	
$V_{\mathrm{core}} = 7.148\ \mathrm{cm}^3$	$\rho = 7.18\ \frac{\mathrm{g}}{\mathrm{cm}^3}$	
$\mu_{\mathrm{r(init)}} = 100$	$OD = 39.9\ \mathrm{mm}$	
$ID = 22.2\ \mathrm{mm}$	$HT = 9.53\ \mathrm{mm}$	

Table 5: The MP4010MPFC's parameters

AC flux swing can push core loss beyond the permissible threshold. Stack two cores to keep the loss within the permissible range. Note that this will double the power handling capacity.

Number of turns in the boost inductance winding:

$$N = \sqrt{\frac{L(\mu H) * 10^3}{A_L}} = \sqrt{\frac{476\ *\ 10^3}{2\ *\ 94}} =\ 50\ turns$$

The maximum DC magnetizing force H for assessing effective permeability μ_e at peak inductor current:

$$H = \frac{I_{L(max)} * N}{l_m} = \frac{8.82\ A * 50\ turn}{9.76\ cm} = 4518\ \frac{A * turn}{m} = 57\ Oersted$$

Measuring permeability against the DC bias curve, the initial value decreased ~12% at peak inductor current. Effective permeability is then $\mu_e = \mu_{r(init)} * 88\% = 88$ and the choke inductance can be recalculated at maximum DC bias. As μ_e decreases, A_L decreases proportionally.

$$L = \frac{N^2 * \mu_0 * \mu_e * A_{core}}{l_m} = \frac{50^2 * (4\pi * 10^{-7}) * 88 * 1.46\ cm^2}{9.76\ cm} = 414\ \mu H$$

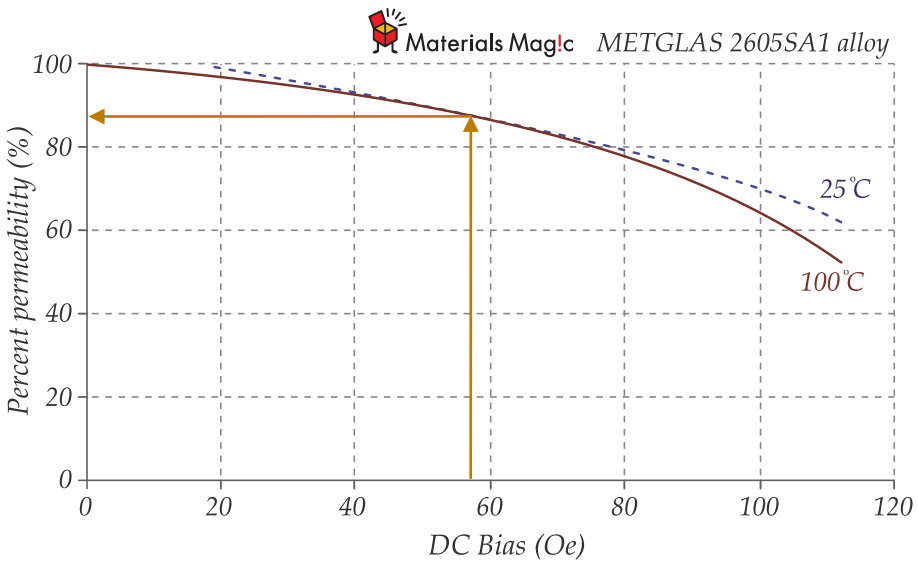


Figure 16: Permeability change as a function of DC bias

Either the higher ripple current resulting from lower inductance is accepted or a new number of turns for the desired inductance is to be calculated:

$$N_{corrected} = \frac{N_{init}}{\frac{\mu_e}{\mu_{r(init)}}} = \frac{50}{\frac{88}{100}} = 57\ turns$$

Lower inductance is somewhat beneficial at diode turn-off because higher ripple current results in lower diode turn-off current and lower reverse recovery loss.

Maximum flux density is attained at the line peak. Saturation can occur when the core flux density B_{max} exceeds the core saturation flux density B_{sat}. The maximum flux density is:

$$B_{max} = \frac{I_{L(max)} * N * A_L}{A_{core}} = \frac{8.82\ A * 57 * 188\ \frac{nH}{N^2}}{1.46\ cm^2} = 0.65\ T$$

Core saturation does not occur because $B_{max} < B_{sat}$ (0.65 T < 1.56 T).

2.3 Windings

It is advisable to minimize the boost inductor's stray capacitance, the distorted waveform of which can affect the inductor's performance. Leakage current caused by stray capacitance can lead to EMI issues.

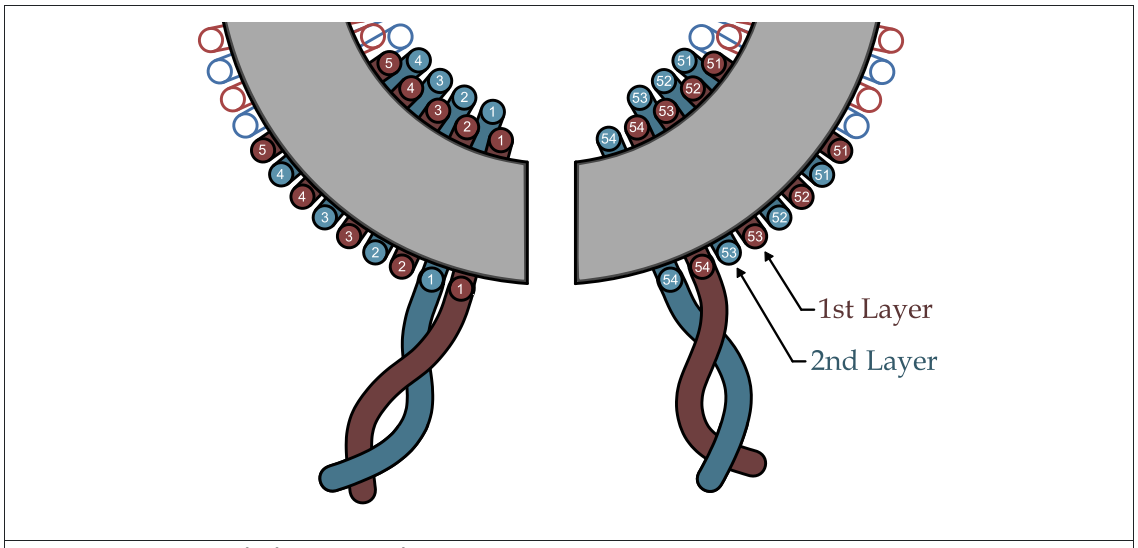


Figure 17: Boost choke wiring diagram

The two layer-winding is made up of 0.8 mm diameter wires. Layers are connected in parallel. A double-layer winding's effective cross-section is larger than that of a single wire, and therefore reduces skin-effect loss at high frequencies.

2.4 Output capacitor selection

Capacitors may be selected with output ripple voltage or the hold-up time requirement in mind. Given a specified 20 ms hold-up time and 300 V minimum output voltage, the capacitance is:

$$C_{out(min)} = \frac{2 * P_{out} * \Delta t}{V_{out}^2 - V_{out(min)}^2} = \frac{2 * 1000\ W * 20\ ms}{400\ V^2 - 300\ V^2} = 571\ \mu F$$

A standard 560 µF, 450 V capacitor is selected as the output capacitor.

The output ripple on the DC link is:

$$V_{o(ripple)} = \frac{I_o}{2 * \pi * f_{line} * C_{out}} = \frac{2.5\ A}{2 * \pi * 50\ Hz * 560\ \mu F} = 14.2\ V$$

2.5 High-frequency input capacitor selection

This capacitor furnishes high-frequency ripple inductor current and minimizes the AC input's high-frequency current requirement. This filters out the noise injected back into the AC input.

The ripple on the input current is inversely proportional to the capacitor value. A high-value capacitor minimizes the noise routed back into the AC input, but a big capacitor also distorts the sinusoidal input current. A standard 470 nF 305 V capacitor was selected as the input capacitor for this application.

3 Measurement and protection circuits

3.1 Temperature measurement

An NTC thermistor is located on the module substrate for temperature measurement. It has a time constant, so it takes a few seconds to detect a change in temperature on a substrate. Because of its slow response, the NTC thermistor is only suitable for protecting the module from slow thermal overrun and not for short-circuit or over-current protection.

The NTC thermistor used in the P95x-A40 has the following characteristics:

Symbol	Parameter	Value	Unit
R_{25}	Resistance @ 25°C (+/-5%)	22	kΩ
$B_{25/85}$	B-constant (25-85°C)	3987	K
I_{op}	Permissive operating current	300	µA
C	Thermal dissipation constant	2	mW/°C

Table 6: NTC thermistor characteristics

To hold the thermistor's self-heating to less than 1 °C, the current on the NTC must be set to lower than I_{op}. The NTC thermistor's resistance at 100 °C is:

$$R_{100} = \frac{R_{25}}{e^{B_{25/85}*\left(\frac{1}{T_{25}}-\frac{1}{T_{100}}\right)}} = \frac{22\ k\Omega}{e^{3987\ K*\left(\frac{1}{298.15\ K}-\frac{1}{373.15\ K}\right)}} = 1.5\ k\Omega$$

At a 5 V supply voltage, the divider resistance has to be set to around:

$$R_{div} = \frac{5\ V}{300\ \mu A} = 16.6\ k\Omega$$

When R_{top} to 15 kΩ is selected, the permissible operating current is around 300 µA at 100 °C. From -55 °C to 125 °C, the output voltage specified for the TEMP output signal lies is 0 V to 2 V. Therefore, an R_{bottom} resistor is needed to limit the voltage to 2 V at low temperature.

Select R_{bottom} to 10 kΩ.

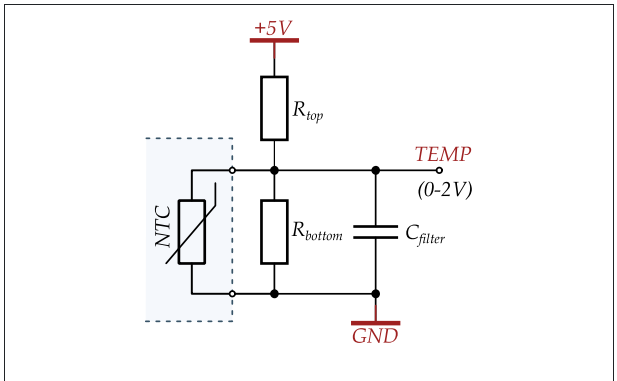


FIGURE 18: THE TEMP SIGNAL

A filter capacitor C_{filter} arrayed in parallel with the NTC thermistor is recommended for boosting the circuit's resistance to noise. A 100 nF filter capacitor provides good noise immunity. The circuit's time constant is $(\tau=\{R_{\text{top}} \times R_{\text{bottom}}\}*C_{\text{filter}})$ and therefore far lower than the NTC thermistor's time constant.

The TEMP voltage is a function of substrate temperature:

$$V_{TEMP} = \frac{R_{bottom} \times R_{NTC}}{R_{top} + (R_{bottom} \times R_{NTC})}$$

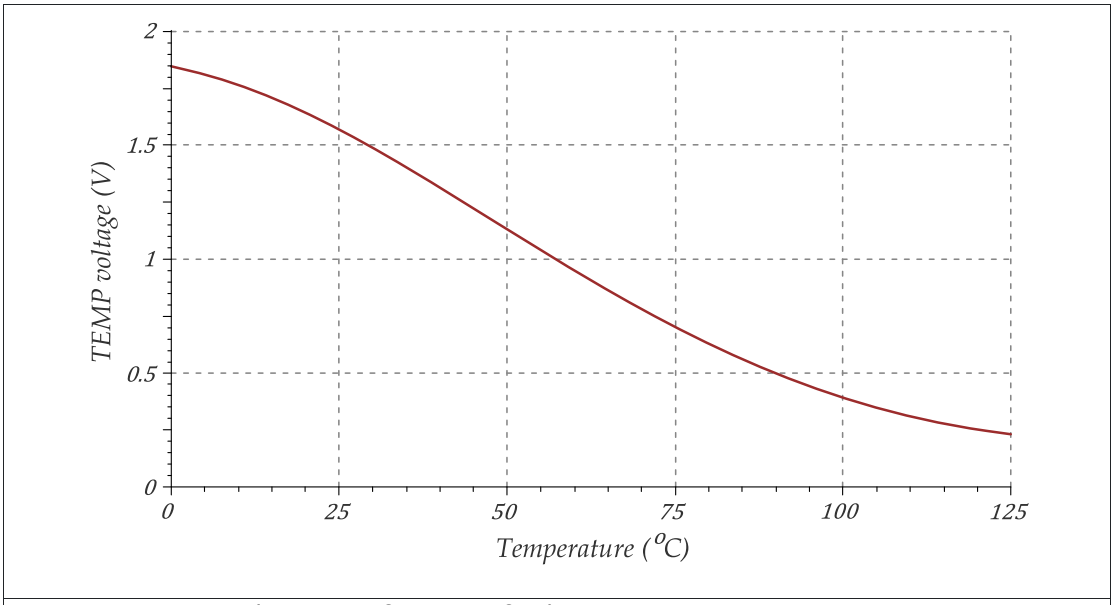


Figure 19: TEMP voltage as a function of substrate temperature

3.2 Over-temperature protection (OTP)

Over-temperature protection is provided by comparing the voltage at the TEMP output to a reference voltage. An NTC thermistor is sited at the bottom leg of the voltage divider (see Figure 18), so the TEMP voltage decreases as the module's temperature increases. The following circuit serves to protect against over-temperature:

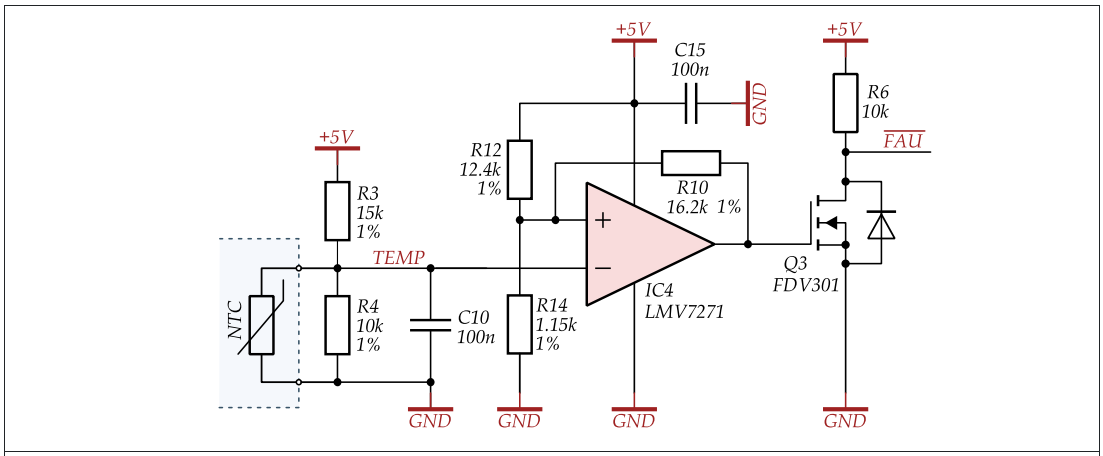


Figure 20: Over-temperature protection circuit

When the TEMP voltage drops below the IC4 comparator 400 mV threshold (V1 threshold) caused by a temperature rise, the comparator changes states, pulls down the $\overline{\text{FAU}}$ line, and shuts down the inverter. Then the fault-latch circuit (see Figure 24) stores and indicates the fault state (via the D3 LED). The inverter can be enabled when the TEMP voltage is beyond the 700 mV threshold (V2 threshold) with a pulse at the RESET input or by pressing the B1 button. The selected thermal protection activation threshold is 100 °C (400 mV) for disabling the inverter and 75 °C (700 mV) for enabling it. See figure 21 for more on this.

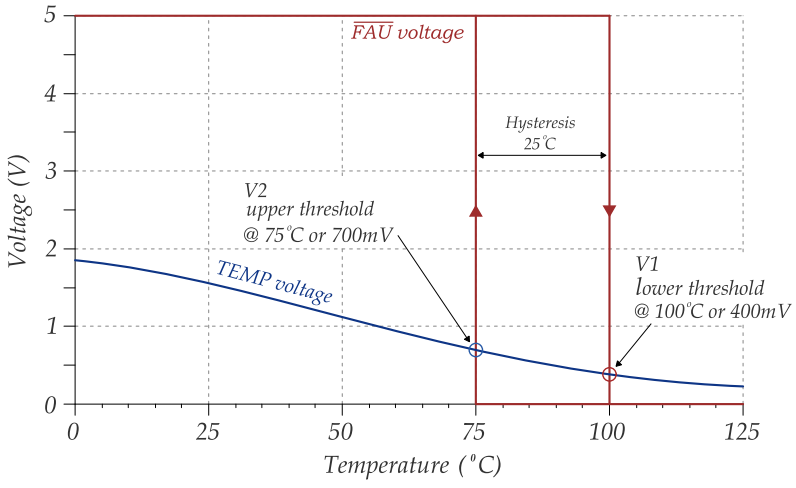


Figure 21: Over-temperature protection transfer characteristic

The resistors in figure 20 could be calculated by applying Kirchhoff's Current Law to their common node:

$$\begin{cases} \dfrac{V_{cc}-V1}{R12}-\dfrac{V1}{R10}=\dfrac{V1}{R14} \\ \dfrac{V_{cc}-V2}{R12}+\dfrac{V_{cc}-V2}{R10}=\dfrac{V2}{R14} \end{cases}$$

There are two equations and three unknowns; choose R10 and express R12, R14:

$$R12=\frac{R10*(V2-V1)}{V1}$$

$$R14=\frac{R10*R12*V1}{R10*(V_{cc}-V1)-R12*V1}$$

Select R10 to 16.2 kΩ; then

$$R12=\frac{R10*(V2-V1)}{V1}=\frac{16.2\,k\Omega*(0.7\,V-0.4\,V)}{0.4\,V}$$
$$=12.15\,k\Omega, \qquad select\ 12.4\,k\Omega$$

$$R14=\frac{R10*R12*V1}{R10*(V_{cc}-V1)-R12*V1}=\frac{16.2\,k\Omega*12.4\,k\Omega*0.4\,V}{16.2\,k\Omega*(5\,V-0.4\,V)-12.4\,k\Omega*0.4\,V}$$
$$=1.15\,k\Omega$$

3.3 Voltage measurement and over-voltage protection (OVP)

The DC link voltage is measured directly using a resistive divider consisting of R8, R11, R13, and R16. The 450 V DC link voltage corresponds to 2 V DCV (divide factor: 1/225). The divided voltage DCV is routed to pin 3 on connector P1.

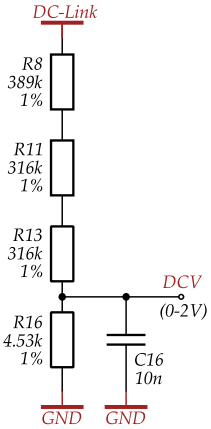


Figure 22: DC link divider circuit

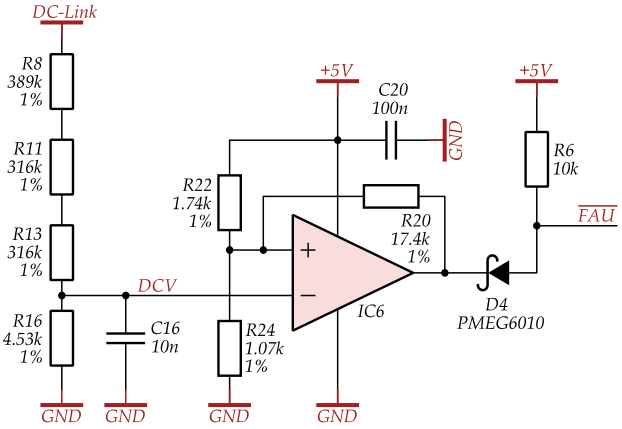


Figure 23: Over-voltage protection circuit

When the inverter reduces its output frequency to decelerate the load, the motor can temporarily become a generator. This occurs when the motor rotation frequency is higher than the inverter output frequency and causes the DC link voltage to rise, resulting in an over-voltage condition. This EVA board lacks a brake circuit, so the external control circuit has to monitor the DC link voltage via the DCV output and set an appropriate output frequency that does not cause the DC link voltage to rise. The over-voltage protection circuit can serve as a safeguard against DC link voltage when it rises above 450 V in case of using an asynchronous motor. At a value higher than 450 V, the IC5 comparator pulls the $\overline{\text{FAU}}$ line down and shuts off the inverter so the asynchronous motor cannot feed back energy to the DC link.

3.4 Fault latch circuit

This is a fast-responding fault latch circuit. A fault signal can be triggered by over-current, over-temperature or over-voltage. In this case, the $\overline{\text{FAU}}$ line is pulled down and the D-type's asynchronous clear input ($\overline{\text{CLR}}$) flip-flops. When the $\overline{\text{CLR}}$ input is low, the Q output is forced into a low state regardless of the clock input and disables the inverter. The D3 LED indicates the fault condition. The input remains flip-flopped until an inbound clock signal arrives at the CLK input. Apply a 1 µs pulse to the RESET input on the P2 connector to generate a clock signal and enable the inverter. Pressing the B1 button resets the circuit as well.

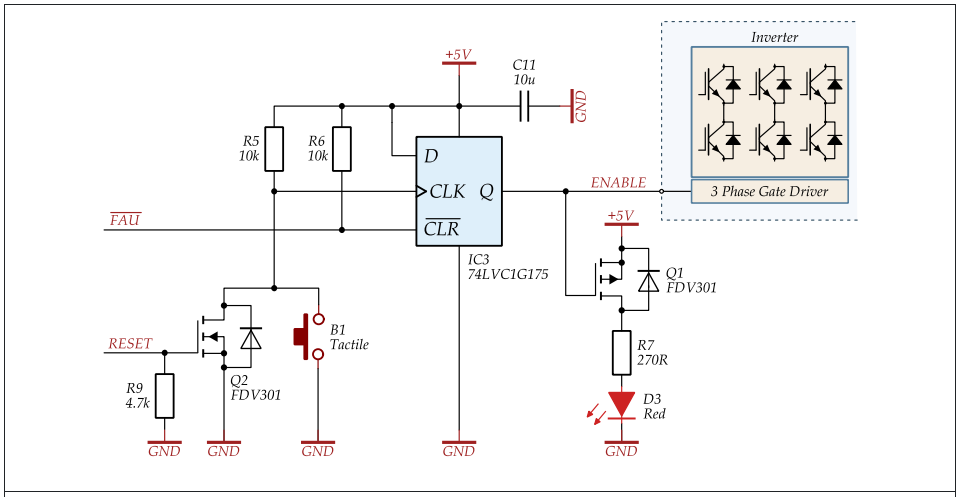


Figure 24: Fault latch circuit

4.1 DC link current measurement

The InvS+ and InvS- pins are connected directly to the inverter shunt in the IGBTs' common low-side path. A differential amplifier is connected to these pins to measure the DC link current. The amplifier has a first-order LPF to filter out switching noise and average the $I_{DC\ link}$. The differential bandwidth (BW_{DIFF}) defines the filter's frequency response with a differential input signal applied between the circuit's two inputs (InvS+ and InvS-).

$$BW_{DIFF} = \frac{1}{2 * \pi * (R19 + R21) * \left(\frac{C19}{2}\right)} = 490\ Hz$$

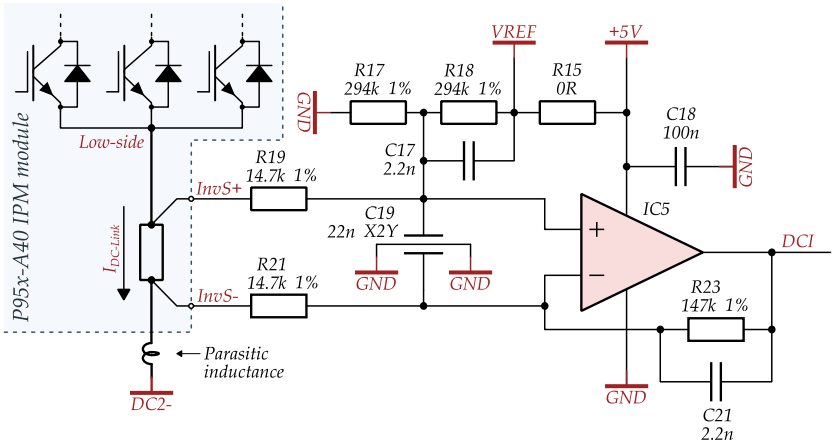


Figure 25: The current sense circuit

The differential amplifier is set to a gain of 10. The current measurement ratio is the voltage change at the DCI output divided by the current change at the inverter shunt ($\Delta V_{DCI}/\Delta I_{DC\ link}$).

Module name	Nominal current	DC link shunt	Measurement ratio	Current range
P952-A40	4 A	50 mΩ	500 mV/A	±5 A
P955-A40	10 A	25 mΩ	250 mV/A	±10 A

Table 7:

The output voltage at the DCI is boosted to accommodate positive and negative current swings. R15, R17 and R18 are populated by default, so the DCI output is boosted by 2.5 V. As a result, the maximum current that can be measured by a 5 V A/D converter is ±5 A and ±10 A. You may apply 'custom' external offset voltage to the P2 connector's pin 7 (OFFSET). Do not populate R17 and R15 resistors when using external offset voltage and be sure to change R18 to 147 kΩ. The LPF input uses an X2Y capacitor for C19 to minimize the mismatch

between the time constants of R19/C19 and R21/C19. This capacitor's tolerance is very tight and helps to suppress common mode noise resulting from the conversion to differential mode.

5 Test results

Figure 26 depicts the general PFC waveforms at 200 V_{RMS} input voltage and 1 kW output power. The PFC converter operates in continuous conduction mode (CCM). The inductor ripple current comes to around 20%. The circuit skips cycles near the line-zero crossing where power transfer is particularly inefficient.

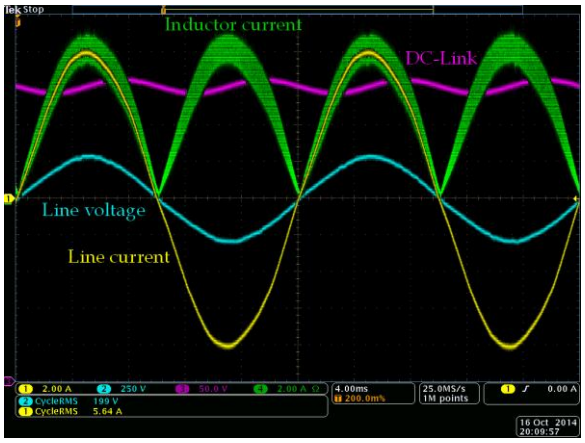


Figure 26: General PFC waveforms at full load (Vin = 200 VRMS, Pout = 1000 W)

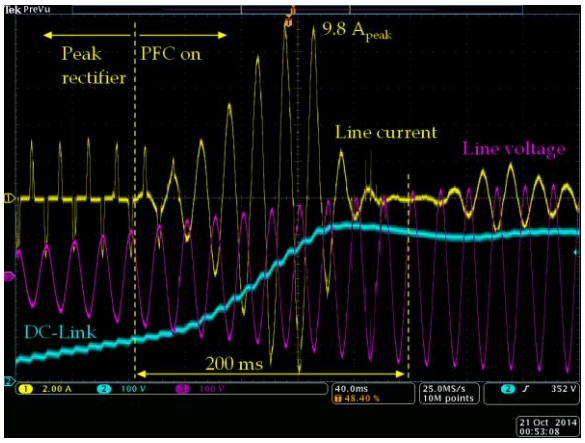


Figure 27: PFC startup with a slow input voltage increase (startup threshold = 75 VRMS)

Insufficient input voltage jeopardizes the PFC's operation. Overheating may occur if the input voltage is lower than the specified 85 V_{RMS}. Brownout protection is needed to shield the circuit from unsafe operation. It is provided in the P95x-A40 by sensing the DC link voltage. When the DC link voltage is lower than 20% of its rated value, the module inhibits the PFC's operation. This means the module has the following level of brownout protection at the 400 V DC link: $V_{\mathrm{BrownoutTH}} = 400\ \mathrm{V} * 20\ \% / \sqrt{2} = 56\ \mathrm{V_{RMS}}$

Figure 27 shows brownout protection with a slow input voltage increase. The PFC's operation is enabled at 75 V_{RMS} because this is the brownout protection level of the IC2 onboard power supply that furnishes 15 V to the module.

The P95x-A40 senses the current flow through the PFC power switch using an integrated current sense resistor. In the P955-A40 module, a peak current limit (PCL) comparator connected to the current sense signal clamps the inductor current at 10 A_{peak}. Figure 28 shows an over-current scenario when the PCL comparator is activated.

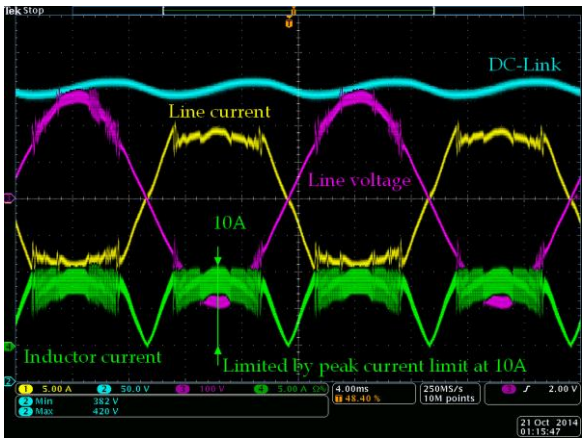


Figure 28: PFC over-current situation (Vin = 200 VRMS, Pout = 1600 W)

Figures 29 and 30 show PFC startup waveforms. The P95x-A40 uses a soft-start to reduce inrush energy at startup. The average current of the PFC choke increases linearly from zero to maximum (limited by PCL). The DC link voltage settles in 140 ms at 200 V_{RMS} input and 320 ms at 100 V_{RMS} input (at half load condition).

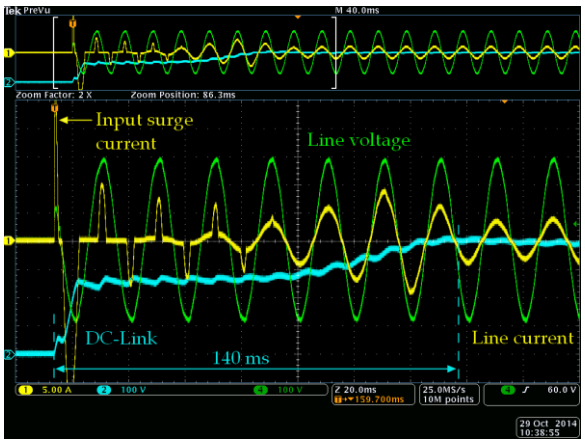


Figure 29: Startup at half load (Vin = 200 V, Pout = 500 W)

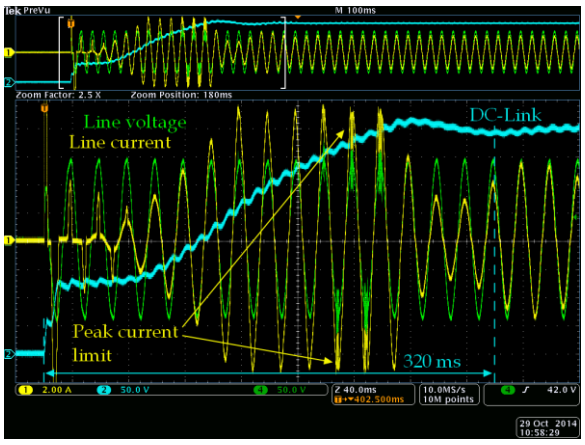


Figure 30: Startup at half load (Vin = 100 V, Pout = 250 W)

Figures 31 to 34 depict the PFC stage's dynamic performance. The undershoot on the DC link is 72 V when the load jumps from no load to full load at 200 V_{RMS} input voltage (figure 31). The input current shows some PCL-driven distortion during the load jump.

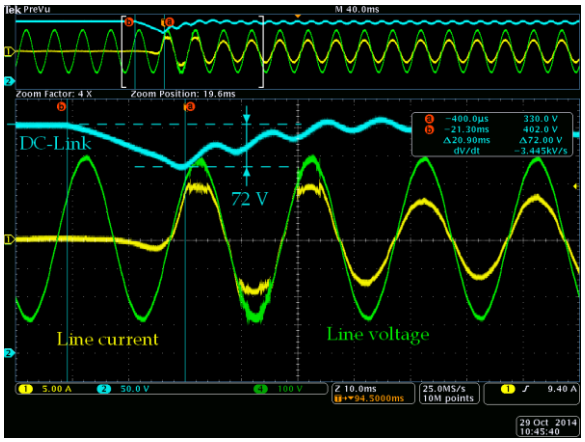


Figure 31: Load jump
(V_{in} = 200 V, P_{out} from 0 W to 1000 W)

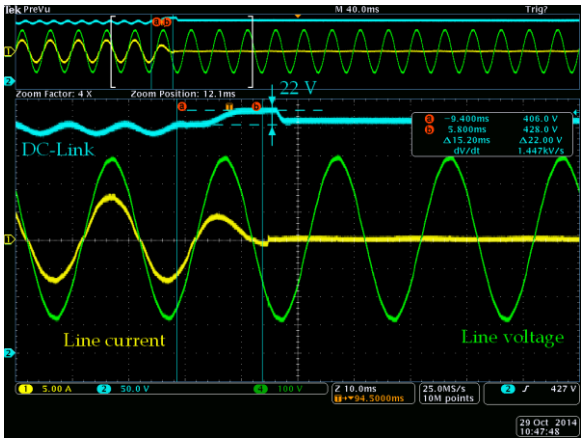


Figure 32: Load jump
(V_{in} = 200 V, P_{out} from 1000 W to 0 W)

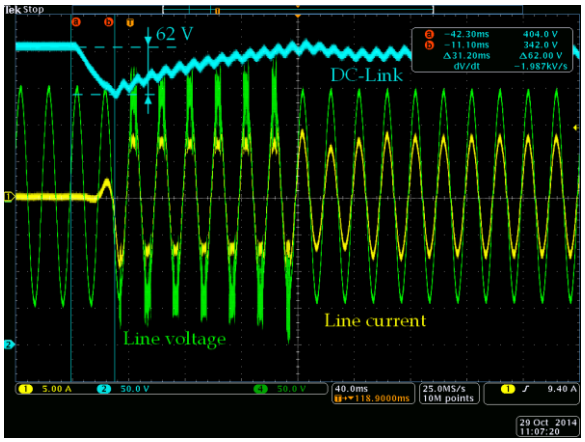


Figure 33: Load jump
(V_{in} = 100 V, P_{out} from 0 W to 500 W)

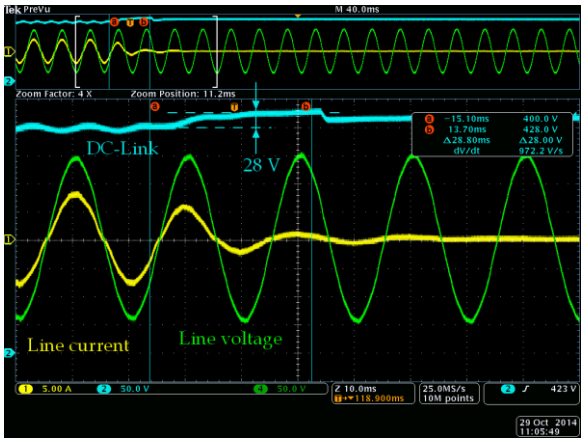


Figure 34: Load jump
(V_{in} = 100 V, P_{out} from 500 W to 0 W)

5.1 Harmonic current

The following table indicates the test limits for harmonic currents according to the EN 61000-3-2 Class A standard.

Harmonic order (A)	Maximum permissible current (A)
3	2.30
5	1.44
7	0.77
9	0.40
11	0.33
13	0.21
15 ≤ n ≤ 39	0.15 x 15 / n

Table 8: EN 61000-3-2 Class A standard current limits

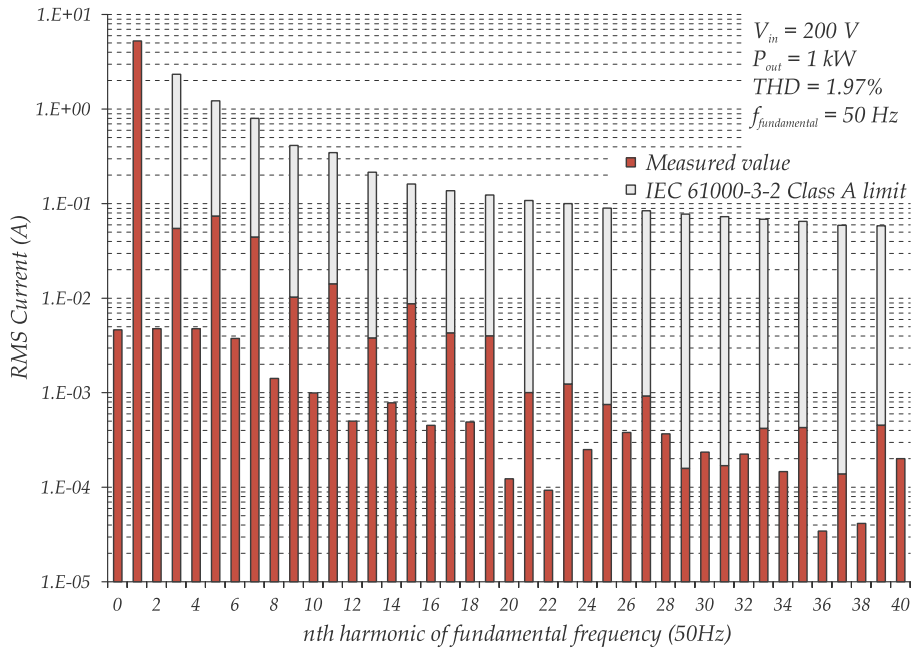


Figure 35: Current harmonics at 200 V_{RMS} input and 1kW load

5.2 Efficiency and power factor

As shown in tables 10 to 12, the power factor at 100% load, 50% load and 10% load remains above 0.95 over the entire specified input voltage range. The measured efficiency shown in figure 36 is always greater than 90% at full load and the peak efficiency is 96.81%. These measurements were taken without the R2 resistor and with a shorted NTC.

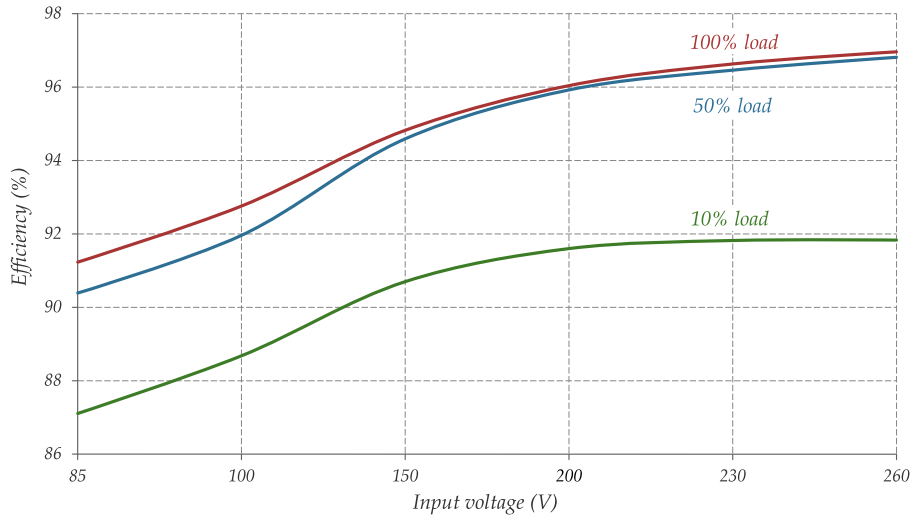


Figure 36: PFC efficiency at various loads

V_{in} [V]	P_{in} [W]	P_{out} [W]	Power factor	Efficiency [%]
85	472.0	426.68	0.9990	90.39
100	545.1	501.30	0.9992	91.96
150	795.2	752.2	0.9994	94.59
200	1046.8	1004.1	0.9993	95.92
230	1193.2	1151.0	0.9990	96.46
260	1349.8	1306.8	0.9988	96.81

Table 9: Efficiency and PF at 100% load

V_{in} [V]	P_{in} [W]	P_{out} [W]	Power factor	Efficiency [%]
85	232.46	212.07	0.9983	91.23
100	270.18	250.63	0.9985	92.76
150	396.1	375.58	0.9989	94.82
200	521.0	500.35	0.9987	96.04
230	595.8	575.7	0.9985	96.63
260	672.0	651.6	0.9979	96.96

Table 10: Efficiency and PF at 50% load

V_{in} [V]	P_{in} [W]	P_{out} [W]	Power factor	Efficiency [%]
85	48.57	42.31	0.9918	87.11
100	57.51	51.00	0.9945	88.68
150	84.15	76.36	0.9872	90.74
200	109.12	100.16	0.9776	91.79
230	126.10	115.79	0.9704	91.82
260	142.98	131.30	0.9617	91.83

Table 11: Efficiency and PF at 10% load

6 Dimensions

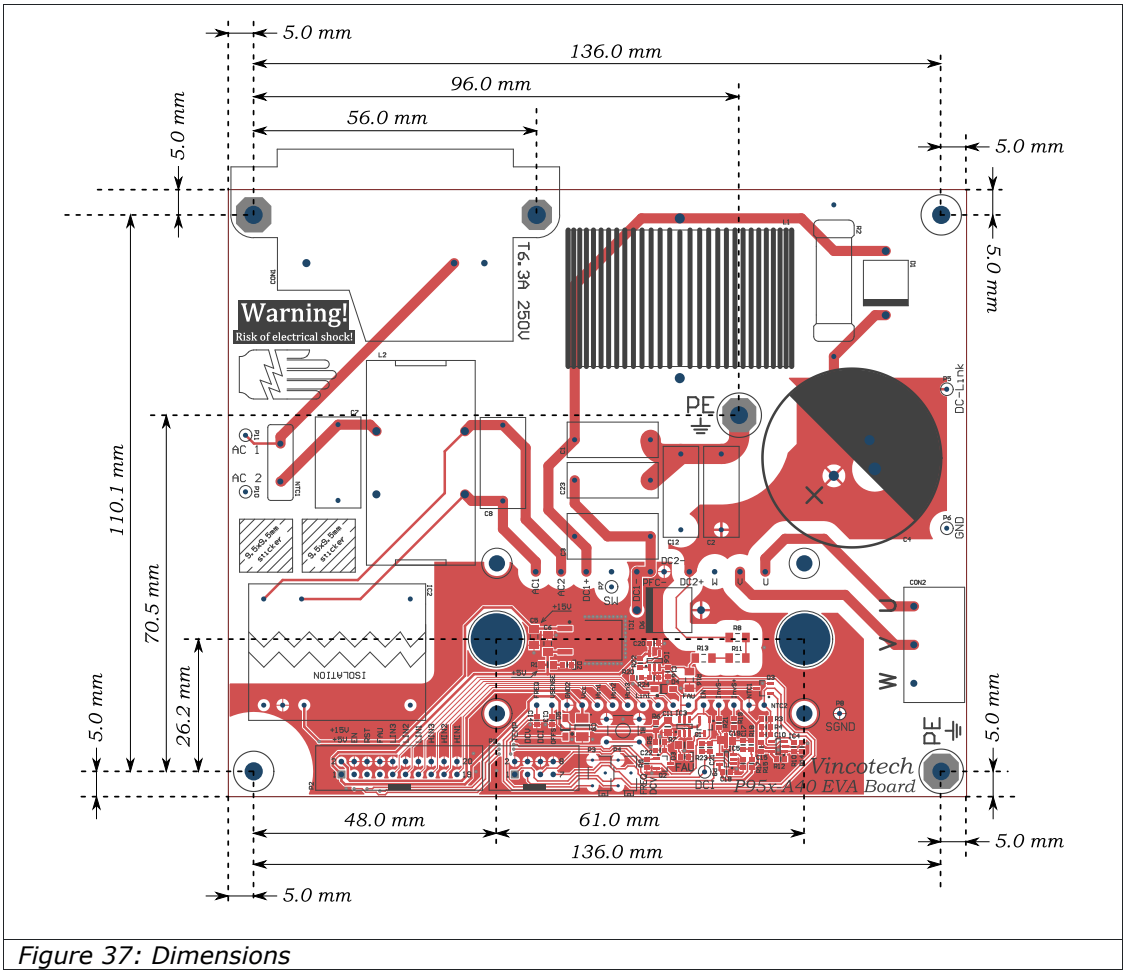


Figure 37: Dimensions

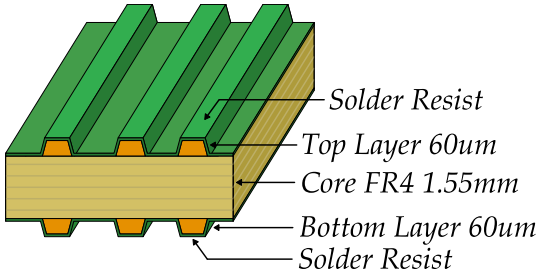


Figure 38: Stacked PCB layers

7 Board layout

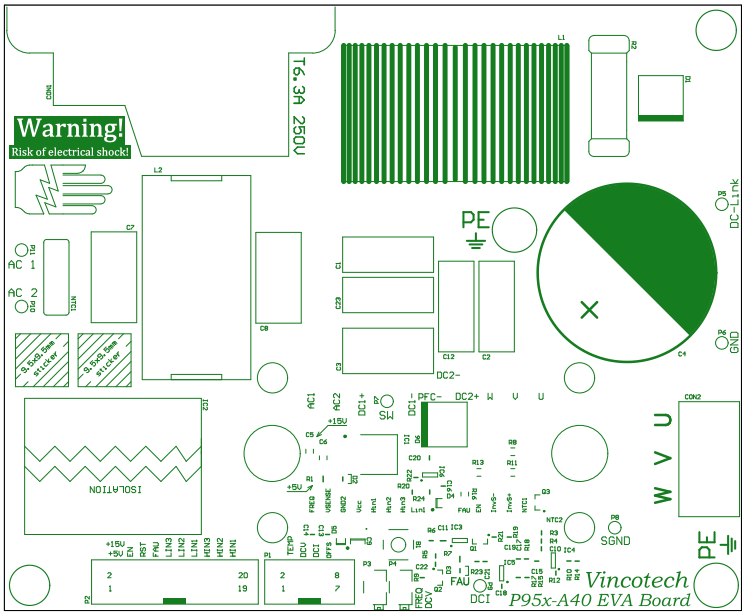


Figure 39: Top silkscreen

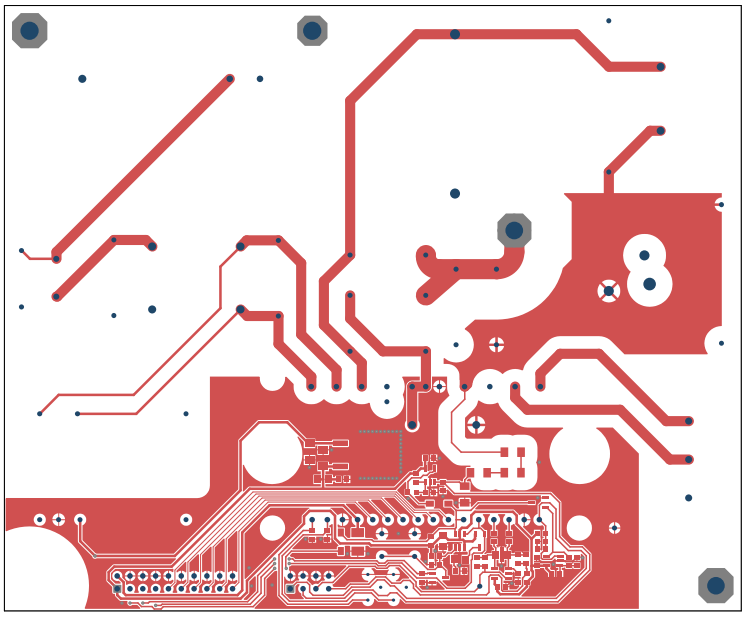


Figure 40: Top layer

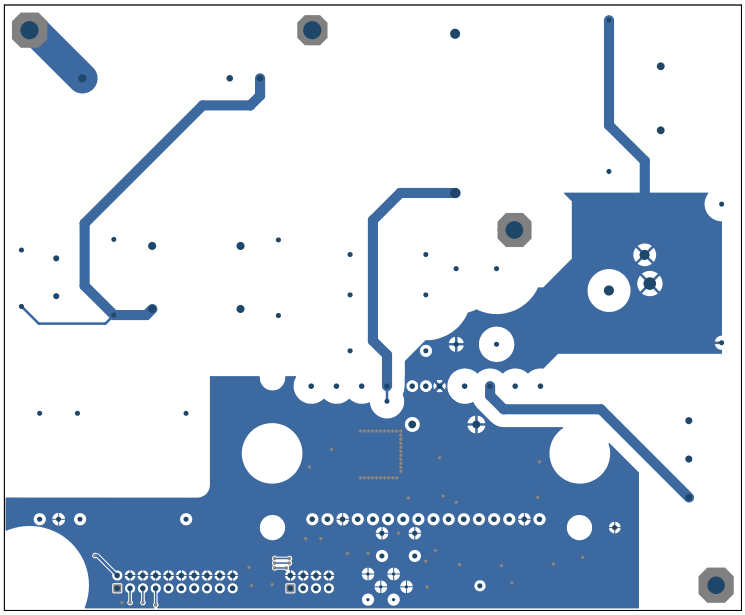


Figure 41: Bottom layer

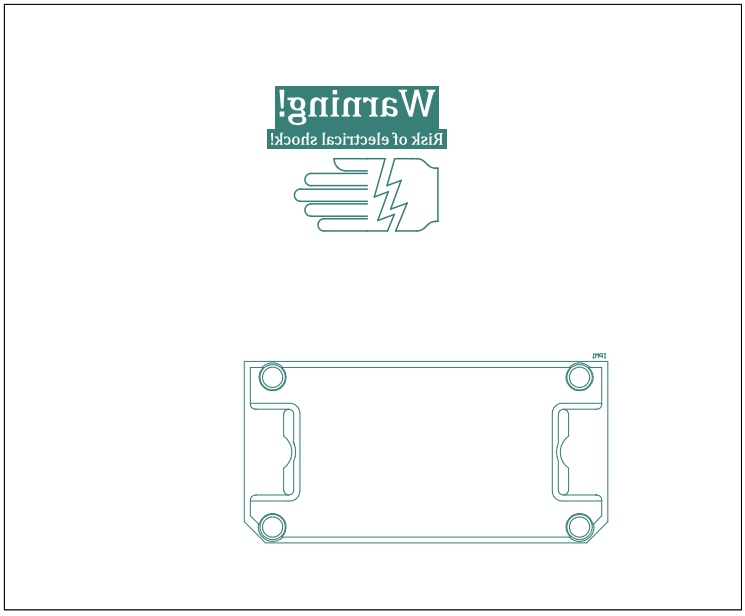


Figure 42: Bottom silkscreen

8 Bill of material

Designator	Part type	Manufacturer/part number	Qty	Supplier	Part number
B1	Tactile Button	SCHURTER - 1301.9307	1	Farnell	1217777
C1, C2, C12, C23	Film Capacitor, 2.2n, 250V, Y1	EPCOS - B81123C1222M	4	Farnell	9751491
C10, C15, C18, C20	SMD Capacitor, X7R, 0603, 100n, 50V	MURATA - GRM188R71H104KA93D	4	Farnell	8820023
C11	SMD Capacitor, X5R, 0805, 10u, 16V	MURATA - GRM219R61C106KA73D	1	Farnell	1845747
C13, C14, C22	SMD Capacitor, NP0, 0603, 1n, 100V	MURATA - CGA3E2C0G2A102J080AA	3	Farnell	2210862
C16	SMD Capacitor, NP0, 0603, 10n, 50V	TDK - C1608C0G1H103J080AA	1	Farnell	1907314
C17, C21	SMD Capacitor, NP0, 0603, 2.2n, 50V	MURATA - GRM1885C1H222JA01D	2	Farnell	8819947
C19	X2Y SMD Capacitor, X7R, 0805, 22n, 50V	JOHANSON - 500X15W223MV4E	1	Farnell	1886158
C3, C7, C8	Film Capacitor, MKP, 15mm, 470n, 305V, X2	EPCOS - B32922C3474M189	3	Farnell	2291758
C4	Electrolytic Capacitor, 560u, 450V, D35mm	EPCOS - B43540A5567M	1	Farnell	2283959
C5, C6	SMD Capacitor, X7R, 1206, 10u, 25V	MURATA - GRM31CR71E106KA12L	2	Farnell	1828837
C9	SMD Capacitor, Tantalum, Size B, 10u, 25V	AVX - TAJB106K025RNJ	1	Farnell	2333024
CON1	Connector, IEC C14, 250V, 10A, Fused	SCHURTER - DD21.0111.1111	1	Digi-Key	486-1305-ND
CON2	Connector, Base Strip, 400V, 12A	PHOENIX CONTACT- 1728866	1	Mouser	651-1728866
D1, D6	Diode, General Purpose, 600V, 6A	VISHAY - P600J	2	Farnell	1702801
D2	LED, Green, 0603	WÜRTH - 150060VS75000	1	Farnell	2322073
D3	LED, Red, 0603	WÜRTH - 150060SS75000	1	Farnell	2322072
D4, D5	Diode, Schottky, SOD123F, 60V, 1A	NXP - PMEG6010CEH	2	Farnell	1510694
IC1	IC, Voltage Regulator, DPAK, 5V, 500mA	ST - L78M05ABDT-TR	1	Farnell	1366575
IC2	IC, DC/DC Converter, Isolated, 15V, 4W	TRACO POWER - TMLM04115	1	Farnell	1772163

IC3	IC, D Flip-Flop, SOT23-6	TI - SN74LVC1G175DBVT	1	Farnell	1494931
IC4, IC6	IC, Comparator, SOT23-5	TI - LMV7271MF	2	Farnell	9779795
IC5	IC, Operational Amplifier, SOT23-5	TI - OPA364AIDBVTG4	1	Farnell	1207054
IPM1	IPM Module, flowIPM 1B, 600V, 10A/4A	VINCOTECH - P955-A40, P952-A40	1	Vincotech	
L1	Inductor, 540uH, 6A	HITACHI METALS - MP4010MPFC	2	Hitachi Metals	
L2	Inductor, Common Mode, 3.9mH, 6A	EPCOS - B82725J2602N020	1	Farnell	1644821
NTC1	NTC thermistor, 5R, 6.4A	EPCOS - B57238S509M	1	Farnell	1704471
P1	Connector, Box Header, 8 way	AMPHENOL - T821108A1S100CEU	1	Farnell	2215303
P2	Connector, Box Header, 20 way	AMPHENOL - T821120A1S100CEU	1	Farnell	2215309
P3, P4	Trimmer Potentiometer, 200k	BOURNS - 3266X-1-204LF	2	Farnell	9352856
P5, P9	Test Pin, Red	MULTICOMP - TEST-1(R)	2	Farnell	1701997
P6, P8	Test Pin, Black	MULTICOMP - TEST-1(BK)	2	Farnell	1702000
P7, P10, P11	Test Pin, Blue	MULTICOMP - TEST-1(BU)	3	Farnell	1701999
Q1	MOSFET, P-ch, -50V, -130mA, SOT23	FAIRCHILD - BSS84	1	Farnell	2323155
Q2, Q3	MOSFET, N-ch, 25V, 0.2A, SOT23	FAIRCHILD - FDV301N	2	Farnell	9845011
R1, R7	SMD Resistor, 0805, 270R, 1%	WELWYN - WCR0805-270RFI	2	Farnell	1100310
R10	SMD Resistor, 0603, 16.2k, 1%	VISHAY - CRCW060316K2FKEA	1	Farnell	2138434
R11, R13	SMD Resistor, 1206, 316k, 1%	MULTICOMP - MC0125W12061316K	2	Farnell	2142312
R12	SMD Resistor, 0603, 12.4k, 1%	VISHAY - CRCW060312K4FKEA	1	Farnell	1652836
R14	SMD Resistor, 0603, 1.15k, 1%	VISHAY - CRCW06031K15FKEA	1	Farnell	2138355
R15	SMD Resistor, 0603, 0R	Vishay - CRCW06030000Z0EA	1	Farnell	1469739
R16	SMD Resistor, 1206, 4.53k, 1%	VISHAY - CRCW12064K53FKEA	1	Farnell	2139483
R17, R18	SMD Resistor, 0603, 294k, 1%	Vishay - CRCW0603294KFKEA	2	Farnell	2138541
R19, R21	SMD Resistor, 0603, 14.7k, 1%	Vishay - CRCW060314K7FKEA	2	Farnell	1469756
R2	THT Resistor, 82k, 5W, 5%	Panasonic - ERG5SJ823	1	Farnell	2324649

R20	SMD Resistor, 0603, 17.4k, 1%	VISHAY - CRCW060317K4FKEA	1	Farnell	2138436
R22	SMD Resistor, 0603, 1.74k, 1%	VISHAY - CRCW06031K74FKEA	1	Farnell	2138370
R23	SMD Resistor, 0603, 147k, 1%	Vishay - CRCW0603147KFKEA	1	Farnell	2138514
R24	SMD Resistor, 0603, 1.07k, 1%	VISHAY - CRCW06031K07FKEA	1	Farnell	2138352
R3	SMD Resistor, 0603, 15k, 1%	VISHAY - CRCW060315K0FKEA	1	Farnell	1469758
R4, R5, R6	SMD Resistor, 0603, 10k, 1%	Vishay - CRCW060310K0FKEA	3	Farnell	1469748
R8	SMD Resistor, 1206, 383k, 1%	MULTICOMP - MC0125W12061383K	1	Farnell	2142317
R9	SMD Resistor, 0603, 4.7k, 1%	Vishay - CRCW06034K70FKEA	1	Farnell	1469807