



# Product Qualification at Vincotech

## 1. Introduction

The following qualification tests are the minimum requirements for the series release of power modules. These tests also apply for release and re-qualification of modified products.

## 2. Description of qualification tests

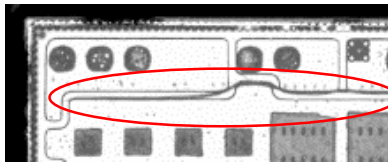
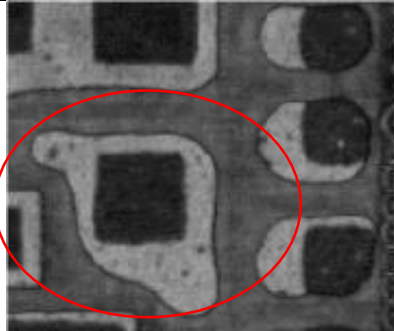
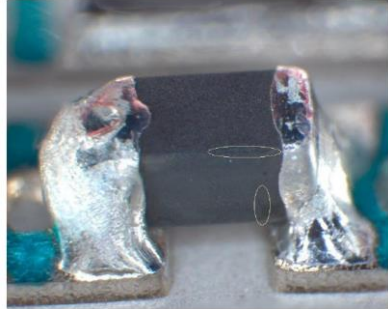

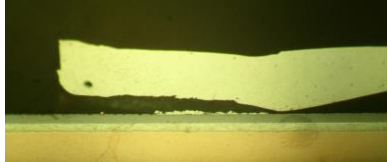
Test name <sup>1</sup>	Conditions <sup>2</sup>	Related standard <sup>6</sup>	Tested failure mode	Acceptance criteria for all test samples
Thermal shock	-40°C (30min), 125°C (30min), 50cycles	IEC 60068-2-14	Substrate fracture	Electrical parameters within spec. limits 6kV isolation test passed SAM passed
			Copper delamination	
			Component fracture	
Power cycling <sup>3</sup>	$\Delta T_{vj}=100^{\circ}\text{C}$ , $T_{\text{max}}=T_{vj, \text{op max}}-25^{\circ}\text{C}$ , Min. 10000cycles	IEC 60749-34	Solder fatigue	$R_{\text{th}}$ incr. <20% $V_f$ incr. <20%
			Bond wire lift-off	
High temperature reverse biased <sup>4</sup>	$T_{vj}=T_{vj, \text{op max}}-25^{\circ}\text{C}$ $V_{\text{DC}}=0.8*V_{\text{max}}$ 1000hrs	IEC 60749-23	Degradation of die passivation	Electrical parameters within spec. limits
High temperature reverse biased <sup>4</sup> (Spec. rectifier diodes)	$T_{vj}=T_{vj, \text{op max}}-25^{\circ}\text{C}$ $V_{\text{peak, half sine}}=0.8*V_{\text{max}}$ 1000hrs			
High humidity high temperature reverse biased <sup>4</sup>	$T_{\text{amb}}=85^{\circ}\text{C}$ , $H=85\text{rH}\%$ , $V=80\text{V}$ , 1000hrs	IEC 60749-5	Degradation of die passivation	Electrical parameters within spec. limits
			Corrosion of metals (die, wire)	
			Electrochemical migration	
Vibration	Sine wave sweep, 20-2000Hz, 1.5mm or 20G, 4min/cycle, 6cycles per axis, X, Y, Z axes	IEC 60749-12	Fatigue fracture	Electrical parameters within spec. limits 6kV isolation test passed
High temperature storage <sup>5</sup>	$T_{\text{amb}} = T_{\text{stg max}}$ , 1000hrs	IEC 60749-6	Shift in electrical parameters	Electrical parameters within spec. limits
High temperature high humidity storage <sup>5</sup>	$T_{\text{amb}}=85^{\circ}\text{C}$ , $H=85\text{rH}\%$ , 1000hrs	IEC 60749-42	Shift in electrical parameters	Electrical parameters within spec. limits

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Notes:

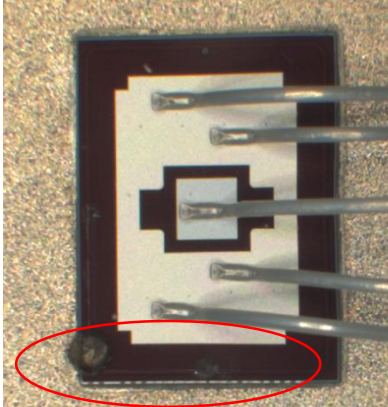
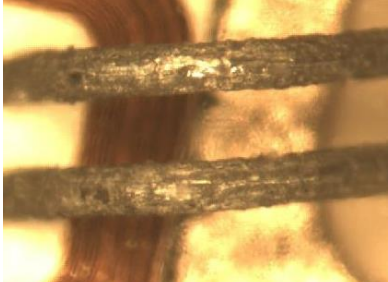
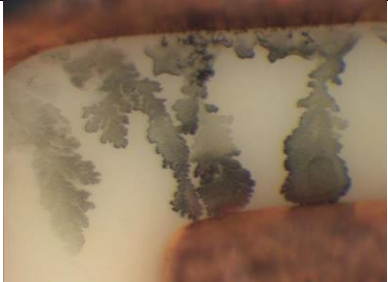

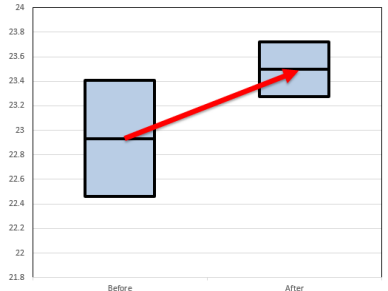
1. This list contains the typical qualification tests. The actual qualification plan for a design change is determined on a case-by-case basis taking into account possible references to already qualified designs.
2. Typical conditions are described here. In special cases tests are run with slightly different conditions.
3. For active components
4. For active components and capacitors; actual voltage and temperature levels are specified by the limitations of the tested components
5. For resistors and thermistors
6. The standards are used as reference, specific test conditions are defined by Vincotech internal regulation

## 3. Tested failure modes and failure mechanisms

Failure mode	Failure mechanism	Example
Substrate fracture	Ceramic substrates must survive any mechanical stress caused by screwing down the power module to the heat sink. Temperature cycling further increases this mechanical stress due to thermal expansion and CTE-mismatch between the different materials. The additional stress may lead to ceramic cracks and loss of isolation.	
Copper delamination	Due to the CTE-mismatch between the copper tracks and the ceramic substrate, copper can delaminate from the ceramic over several hundred thermal cycles causing an increase in the $R_{th}$ value.	
Component fracture	Capacitors, resistors and thermistors can crack and lose functionality due to the thermo-mechanical stress induced by temperature cycling.	
Solder fatigue	Solder joints can degrade during active power cycling test due to mechanical stress caused by various CTE mismatches (i.e. silicon die and copper track or ceramic substrate and copper baseplate). This degradation process can include the growth of brittle intermetallic phases, intermediate voids and solder delamination. Eventually, this will cause a local increase in junction temperature and thermal runaway.	
Bond wire lift-off	Due to the CTE mismatch between the bond wire, the copper track and the silicon die, the wires can lift-off during power cycling test, causing an increase in the forward voltage or a complete loss of electrical connection.	



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<p>Degradation of die passivation</p>	<p>The degradation of die passivation under either high temperature or high humidity and high temperature can cause electrical failure.</p>																			
<p>Corrosion of metals (die, wire)</p>	<p>The corrosion of metals (die metallization or bond wires) under high temperature and high humidity can lead to electrical failure over time.</p>																			
<p>Electrochemical migration</p>	<p>In an environment with high humidity, it is possible for water to condense on the electrical layout, which can lead to dendritic growth between metals of opposite polarity and eventually causing an electrical short.</p>																			
<p>Fatigue fracture</p>	<p>Mechanical stress from vibration can cause fractures in the structural materials leading to loss of functionality or isolation failure.</p>																			
<p>Shift in electrical parameters</p>	<p>The electrical characteristics of components can shift after long exposure to high temperature and/or high humidity due to oxidation, corrosion or intermetallic growth.</p>	 <table border="1"><caption>Box Plot Data</caption><thead><tr><th>Parameter</th><th>Min</th><th>Q1</th><th>Median</th><th>Q3</th><th>Max</th></tr></thead><tbody><tr><td>Before</td><td>22.4</td><td>22.5</td><td>22.8</td><td>23.4</td><td>23.8</td></tr><tr><td>After</td><td>23.3</td><td>23.4</td><td>23.5</td><td>23.7</td><td>23.8</td></tr></tbody></table>	Parameter	Min	Q1	Median	Q3	Max	Before	22.4	22.5	22.8	23.4	23.8	After	23.3	23.4	23.5	23.7	23.8
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